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TED KOON HOO

Date of Birth — Date de naissance	Country of Birth — Lieu de naissance
29th NOV. 1953	Singapore

Permanent Address — Résidence fixe

117, Joo Chiat Place,
Singapore 1544
Republic of Singapore

Title of Thesis — Titre de la thèse

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1985	Dr. Gould, Dr. Englefield

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ERROR MECHANISMS AND CLOCK RECOVERY IN FOUR-LEVEL PWM OPTICAL FIBER SYSTEMS

by

KOON HOO TEO

A THESIS

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The undersigned certify that they have read, and recommend to the Faculty of Graduate Studies and Research, for acceptance, a thesis entitled ERROR MECHANISMS AND CLOCK RECOVERY IN FOUR-LEVEL PWM OPTICAL FIBER SYSTEMS submitted by KOON HOO TEO in partial fulfilment of the requirements for the degree of MASTER OF SCIENCE in ELECTRICAL ENGINEERING.

Paul A. Bond ..... C. Ly. Englefield

Supervisor

.....

Wo-Sang Young

Date 20 December, 1984

ABSTRACT

The error mechanisms in a 4-level PWM optical fiber communication system have been investigated previously[1]. That investigation was based on the theory of noise analysis for an analog PWM system. This theory, here referred to as the "slope theory", relates the timing error to the noise variance at the 'slicing' level and to the slope of the falling edge of the received PWM signal. Experimental measurements described in this thesis have, however, shown some inconsistency between the slope theory and experimental results under the usual operating conditions. This has led to the replacement of the slope theory by a more generally applicable theory, referred to in this thesis as the "amplitude theory". This theory relates received errors to the signal amplitude and noise variance at the instant of sampling. Both theoretical and experimental results have shown that the slope theory generally underestimates the system Bit Error Rate (BER) and that the amplitude theory gives a more accurate evaluation.

The second part of this thesis concerns the optimization of the Phase-Locked Loop (PLL) parameters for clock recovery in a 4-level PWM optical fiber receiver. The choice of a PLL instead of a simple tuned circuit is justified by a theoretical comparison between the two circuits. A second-order PLL was used, in order to allow for the independent adjustment of the three major parameters that affect its performance as a clock recovery device. These three major parameters are: the noise bandwidth, the damping factor, and the loop gain. The independent adjustment of these parameters will conveniently permit the experimental determination of their optimum values and hence their optimum ranges. Experimental results have indicated that these parameters conveniently possess a wide range of values that will give near optimum system BER performance. It was experimentally verified that a high-gain PLL with narrow bandwidth and high damping factor can provide a stable, self-recovered clock signal from the incoming modulated signal. A self-recovered clock 4-level PWM system using a PLL was shown to perform well, with only a slight degradation in terms of system BER performance, compared to the case when the receiver is timed by a master (transmitter) clock directly. This excellent performance is attributed to the strong timing content of a PWM signal and to the inherent properties of narrow bandwidth and small static phase error of the PLL.

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TABLE OF CONTENTS

Chapter		Page
1.	INTRODUCTION	1
	1.1 An Optical Fiber Digital Communication System	2
	1.1.1 The Transmitter	2
	1.1.2 The Receiver	4
	1.2 Thesis Objectives and Organisation	5
2.	ERROR MECHANISMS IN A MULTI-LEVEL PWM SYSTEM	9
	2.1 A 4-level PWM System	10
	2.2 Sources of Receiver Noise	10
	2.2.1 Shot Noise	14
	2.2.2 Thermal Noise	15
	2.2.3 The Gaussian Approximation	17
	2.3 Error Mechanisms	18
	2.3.1 The Amplitude Theory	19
	2.3.2 The Slope Theory	23
	2.3.3 Slope Theory: A Particular Case of the Amplitude Theory	25
3.	EXPERIMENTAL INVESTIGATION OF ERROR MECHANISMS	28
	3.1 The Overall Experimental 4-level PWM System	28
	3.1.1 The Transmitter	28
	3.1.2 The Optical Fiber	31
	3.1.3 The Optical Receiver	31
	3.2 Measurements and Results	35
	3.2.1 BER as a Function of Time Delay	35
	3.2.2 Effect of Varying the Slicing Voltage Level	38
	3.2.3 BER as a Function of Received Optical Power	38
	3.3 Discussion of Results	38
4.	TIMING EXTRACTION AND JITTER	44
	4.1 Introduction	44
	4.2 Existence of Timing Signal	46
	4.2.1 Spectra of Analog PAM, PPM and PWM	46

4.2.2 Advantages of Multilevel PWM for Clock Recovery 53
4.3 Jitter and its Parameters 56
4.3.1 Effects of Jitter 56
4.3.2 Defining Peak-to-Peak Jitter 56
4.3.3 Jitter Parameters 59
4.4 Timing Extraction 66
4.4.1 Tuned Circuit 68
4.4.2 Second-order PLL 70
4.4.3 Comparison of Tuned Circuit and PLL for Clock Recovery 72
5. THE PHASE-LOCKED LOOP 74
5.1 Concepts 74
5.2 The PLL in the Locked Condition 76
5.2.1 First Order Loop 77
5.2.2 Second-order Loop 78
5.3 Linear Tracking 82
5.3.1 Steady State Error 82
5.3.2 Transient Response 84
5.3.3 Steady State Response to a Ramp Frequency Input 89
5.4 Noise Bandwidth 90
5.5 Locking Limits 91
5.6 Seize Frequency 94
6. CLOCK RECOVERY FOR A 4-LEVEL PWM SYSTEM 95
6.1 Timing Extraction for a 4-level PWM System 95
6.1.1 Timing Content of a 4-level PWM Signal 95
6.1.2 Sources of Timing Jitter 96
6.1.3 Optimizing PLL Performance in Clock Extraction 98
6.2 Experimental Configuration for Clock Recovery System 100
6.2.1 Overall Experimental Setup 101
6.2.2 The Timing Extraction Circuit 101
6.2.3 Measurement Result 106
6.2.4 Discussion of Experimental Results 115

7. SUMMARY AND CONCLUSION 117
APPENDIX A 121
APPENDIX B 123
REFERENCES 127

LIST OF FIGURES

Figure		Page
1.1	A basic optical fiber digital communication system.	3
2.1	Block diagram of a 4-level PWM optical fiber communicaion system.	11
2.2	Encoding binary data to a 4-level PWM signal.	12
2.3	Decoding a 4-level PWM signal.	12
2.4	Noise sources at the front end of an optical receiver.	13
2.5	Transimpedance amplifier.	16
2.6	Noise variance changes with signal level.	16
2.7	4-level PWM signals with noise.	21
2.8	Effect of slope and noise on timing error.	24
2.9	Waveform comparing slope theory and amplitude theory.	24
3.1	The experimental 4-level PWM optical fiber communication system.	29
3.2	The transmitter for the 4-level PWM optical fiber communication system.	30
3.3	The decoder for the 4-level PWM optical fiber communication system.	32
3.4	The decision logic schematic.	34
3.5	Timing diagram for the gating pulses.	34
3.6	Decoding the PWM signal.	36
3.7	PWM waveform for a '10' pattern sequence.	36
3.8	BER as a function of time delay (t_3 pulse).	37
3.9	BER as a function of time delay (t_1 pulse).	39
3.10	Effect of noise on BER as a function of 'slicing' level.	40
3.11	Change in the effect of noise on BER as the 'slicing' level increased for various pulse amplitudes.	41
3.12	BER as a function of received optical power.	42
4.1	PAM with RZ format.	49
4.2	Quantized PAM.	54
4.3	Clock signal in 4-level pulse modulation.	55
4.4	Conversion of PWM to constant width pulses.	55
4.5	Sinusoidal jitter modulation.	57
4.6	Zero block in negative half modulation period.	60

4.7 Clock recovery limitation. 61
4.8 Fundamental time domain jitter tolerance limits. 64
4.9 A general timing extraction circuit. 67
4.10 Detection of signal transition in NRZ binary data 67
4.11a The threshold detector converting a sinusoidal waveform to a square wave 71
4.11b Amplitude to phase conversion in an imperfect threshold detector. Production of timing jitter by threshold detector. Threshold, normally at zero amplitude, is offset to 'u'. 71
5.1 A phase-locked loop. 75
5.2 Block diagram of a PLL. 75
5.3 Responses of a first-order PLL 79
5.4 Simple low-pass filter. 79
5.5 A lag-lead filter. 81
5.6 Responses for a PLL with a lag-lead filter. 81
5.7 Second-order loop $F(s)=1/(1+T_1s)$; phase error for a step phase of the input signal. 86
5.8 Second-order loop $F(s)=1/(1+T_1s)$; phase error for a step frequency of the input signal. 86
5.9 Second-order loop $F(s)=(1+T_2s)/T_1s$; phase error for a step phase of the input signal. 87
5.10 Second-order loop $F(s)=(1+T_2s)/T_1s$; phase error for a step frequency of the input signal. 87
5.11 Voltage ouput versus phase difference of a triangular phase detector. 92
6.1 Phase shifting of the rising positive edge. 98
6.2 Schematic of a timing extraction circuit. 102
6.3 The PLL(XR215) and its external connections. 103
6.4 BER vs. product of noise bandwidth and time period. 108
6.5 BER vs. damping factor. 110
6.6 BER vs. PLL free running frequency for various values of PLL gain. 111

6.7 BER vs. received optical power. 112
6.8 A simple pattern generator using a shift register. 113
B1a Random pulse train 124
B1b Autocorrelation of non-periodic part $R_1(\tau)$. 124
B1c Autocorrelation for periodic part $R_2(\tau)$. 124
B1d Sum of $R_1(\tau)$ and $R_2(\tau)$. 124
B1e Energy spectrum. 124

Table 6.1. Effects of bit patttern on clock phase. 114

LIST OF SYMBOLS

p(t)	the light intensity or power
η	the photodetector quantum efficiency
n_0	dark current counts per second
λ	average counts per unit time
M	avalanche mean gain
F_M	noise factor
K	Boltzmann's constant
T	temperature
B	channel bandwidth
k	carrier ionisation ratio
σ_T	square root noise variance at a given signal level
σ_m	square root noise variance at the max. signal level
σ_{th}	square root noise variance at the zero signal level
$V_0(t)_s$	signal voltage level
V_{max}	maximum voltage level
n_t	instantaneous noise amplitude
σ_s	square root noise variance at the 'slicing' level
V_d	'slicing' level voltage
s'	slope of the signal at the 'slicing' level
P_{e_a}	probability of error using the amplitude theory
P_{e_s}	probability of error using the slope theory
$c_\delta(t)$	periodic unit impulse train
f_0	line or pulse repetition frequency
s(t)	signal as a function of time
f_i	jitter modulating frequency
Δf	peak frequency deviation
J_{pp}	peak-to-peak jitter
Q	Q factor of a tuned circuit
L	inductance

C	capacitance
ω	angular frequency
f_r	resonant frequency of a tuned circuit
B_n	noise bandwidth of a PLL
ω_n	natural angular frequency of a PLL
ζ	damping factor of a PLL
K	loop gain of a PLL
$\theta_i(t)$	phase of input signal
$\theta_0(t)$	phase of output signal
K_d	phase-detector gain factor
K_0	VCO gain factor
$\Delta\theta$	step change of input phase
$\Delta\omega$	step change of input frequency
θ_e	static phase error
$\theta_e(t)$	phase error in a PLL loop
F(s)	transfer function of a PLL loop filter
N_0	one sided noise power spectral density.
ω_s	seize frequency of a PLL
τ_n	phase shifting
Q_{eff}	effective Q factor of a PLL

Chapter 1
INTRODUCTION

Optical fiber has become a superior alternative to copper for many applications in telecommunication systems. An essential requirement for the use of any new technology is that it must be cost competitive with existing technology, and/or provide new functions which would have been impossible or impracticable with the existing technology.

As is well known, the amount of information that can be carried by a transmission channel depends on the carrrier frequency of the signal and on the bandwidth of the system. The higher the carrier frequency, the larger the quantity of information that can be transmitted. As the frequency of light is approximately a thousand times that of the shortest radio wave, the potential of the former as a means of transmitting information has long been appreciated[2]. It was not until 1966 that Hockham and Kao[3] pointed out the possibility of achieving low attenuation in optical fiber waveguide at a suitable wavelength in the visible or near infra-red region. An attenuation of 20dB/Km was achieved for single mode fiber in 1970[4] and, in 1972, a value of 4dB/Km was obtained for multimode fiber[5]. Since then, much effort has been expended on achieving still lower attenuation and on increasing the bandwidth. An attenuation of as low as 0.2dB/Km at 1.55um wavelength was recently reported for single mode fiber[6]. Research has also shown that the material dispersion of silica fiber passes through zero in the region of 1.3um, which mean that at that wavelength a very large transmission bandwidth (200 GHz-Km for single mode fiber) can be obtained[7].

Applications of the optical fiber have triggered the development of related system components such as optical sources and detectors. LEDs and lasers diodes with mean life times exceeding 10^5 hours are presently commercially available[8]. However, good LEDs are more reliable than lasers, and are much simpler to operate, because the output power varies only slightly with temperature, hence eliminating the need for output stabilization. Nevertheless, lasers diodes can launch more power into a fiber and have a narrower spectral width than LEDs, making them better suited for long-haul, high rate transmission systems[9].

The inherently large bandwidth of optical fiber makes its use in high bit rate digital communication systems very attractive. Though recent research emphasis has been on single mode fiber because of its potentially higher bandwidth for long-haul applications[10],

multimode fibers have gained early widespread use in digial optical communication due to their reliabilility and economic viabilility.

1.1 An Optical Fiber Digital Communication System

The three parts of an optical fiber communication system as depicted in Fig.1.1, are the optical transmitter, the optical fiber transmission channel and the optical receiver. In a digital optical fiber communication system, the transmitter consists of a data encoder, a source driver and an optical source, while the receiver consists of a photodetector, a linear amplifier and a decoder. The transmission channel could be a single mode or multimode fiber depending on system requirements and cost factor. A repeater is basically a back-to-back receiver-transmitter combination unit. Its function is to regenerate and reshape the signal that has been degraded during transmission over the optical fiber. The repeater spacing depends on the fiber bandwidth and attenuation, the optical source and detector used, and on the data rate and modulation code.

1.1.1 The Transmitter

There are many code formats that may be generated by the encoder to represent the source binary bits of 1s and 0s from the data source. Pulse modulation techniques such as pulse code modulation (PCM), pulse-amplitude modulation (PAM) and pulse width modulation (PWM) are some of the code formats being investigated for use in optical fiber systems[11]. Other codes that are being employed are the biphase pulse code, modified phase keying pulse code and alternate mark inversion pulse code[12]. There are a number of factors to be considered when chosing a code format. They are:

1) The characteristics of the optical source such as linewidth, range of linear operation and the power constraint.

2) The dynamic linear range and bandwidth of the receiver.

3) The timing information of the code format. Code formats which provide sufficient transitions will facilitate the recovery of the clock at the receiver.

4) The need to prevent baseline wander.

5) The need for simplicity of circuit design for both the encoder and decoder.

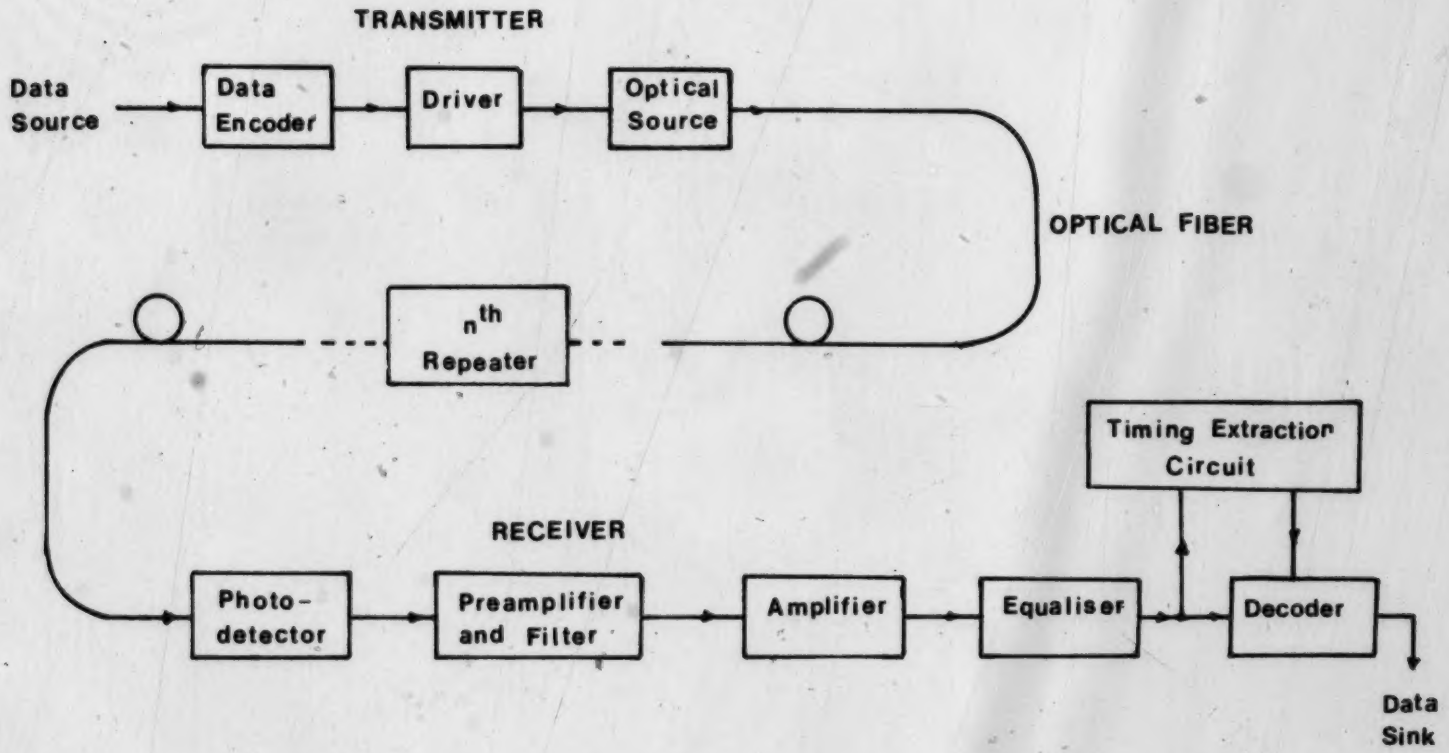


FIG.1.1: A BASIC OPTICAL FIBER DIGITAL COMMUNICATION SYSTEM

Not all codes can meet all of the above requirements. Multi-level PAM might conserve bandwidth but would require a larger linear operating range for both the optical source and receiver. Multi-level PWM, on the other hand requires a broader channel bandwidth, but offers good timing information. Both PWM and PPM have pulses of fixed amplitude, hence they do not suffer from problems due to non-linearity and thermal dependence of the modulation characteristics of the laser diode[13].

The encoded electrical signal controls the driver which modulates the current flowing through the optical source, resulting in the transmitted optical signal. The requirements of an optical source for a high bit rate link are narrow spectral bandwidth, small beam area, high electrical-to-optical power conversion efficiency, high frequency response, long life span and emission of light at wavelengths that are compatible with the optical fiber characteristics.

1.1.2 The Receiver

At the front end of the receiver, the photo-detector converts the optical signal back to an electrical signal. The requirements for this device will be much the same as for the optical source such as high conversion efficiency, frequency response and wavelength compatibility to the source, and additionally a low leakage current and low noise. As the output signal from this detector is normally very small, a low noise preamplifier is used, coupled directly to the photo-detector to amplify the signal level with minimum noise penalty. With a finite level of thermal noise introduced by this preamplifier, an avalanche photodetector is often preferred to a p-i-n diode, in order to achieve higher receiver sensitivity[14].

For a communication channel degraded by white noise, the noise level increases with increasing channel bandwidth. Hence a filter is normally incorporated into the receiver to restrict the noise. The optimum bandwidth of the filter depends on the signal bandwidth, and is chosen to maximise the SNR.

The main amplifier further enhances the signal to a voltage level that is acceptable to the decoder. As the signalling (pulse repetition) rate approaches that of the channel's Nyquist rate, significant intersymbol interference(I.S.I.) could occur. The main function of equalization is to help to neutralise this I.S.I. effect. As the channel bandwidth used in this project was at least twice that of the baud rate which is normally required in a PWM code format, the I.S.I. effect was almost negligible. Hence no equalization circuit was needed in the

receiver used in this project.

At the decoder, the signal must be sampled at precise sampling instants in order to recover the original signal. To perform this sampling, a clock signal is needed at the receiver which is synchronised to the clock signal at the transmitter. This synchronisation can be achieved by having a master clock driving both the transmitter and receiver or, more efficiently by extracting the clock signal from the received signal waveform itself. The complexity of the timing extraction circuit employing the last method depends on the timing information and hence on the code format of the transmitted signal. Non linear signal processing techniques are normally included in a timing extraction unit to more efficiently extract the timing signal from the transmitted message signal[15]. The other major component in a timing extraction unit is the pulse generating and sustaining circuit, for which the two most commonly used circuits are the tuned circuit and the phase locked loop.

1.2 Thesis Objectives and Organisation

A 4-level PWM optical fiber communication system was originally built and successfully tested by Mr Dai Xianda, a visiting scholar from the Beijing Institute of Aeronautics. The main objective of setting up this experimental system was to verify the theoretical evaluation that a multi-level PWM system can achieve very low BER for a given received optical power as compared to multi-level PAM. The theoretical basis for this evaluation, which is referred to in this thesis as the slope theory, is based on the principle that the effect of channel noise on the system BER is dependent on the slope of the falling edge of the PWM signal pulse. The steeper this slope, the smaller will be the effect of noise and hence the better will be the BER performance[1]. Due to time limitations, Mr. Dai did not complete the experiment to verify the slope theory and this task was continued by the author. Some small modifications were made to the experimental set up to allow for more experimental flexibility and an improved system performance. Some elaborate experiments were carried out and it was later found that the above slope theory could be applied only under certain operating conditions. In comparison to the slope theory, another theory, referred to as the amplitude theory in this thesis, has proven to be a more generally applicable theory in predicting the error mechanisms in a multi-level PWM system. Similar to the case of binary PCM, the amplitude theory relates BER to both the signal pulse amplitude (rather than slope) and the noise

variances at the signal 'ON' and signal 'OFF' levels. In both the experimental results and the theoretical evaluation, the amplitude theory shows that the slope theory can greatly underestimate the BER of a multi-level PWM system. Nevertheless, experimental results have shown that a 4-level PWM system still does perform well; a BER of 10^{-9} for a received optical power of approximately 1 nW, operating at a bit rate of 5Mbit/s.

With the experimental verification of the validity of the amplitude theory, the multi-level PWM system is seen to have no significant advantage over multi-level PAM with respect to system BER[16]. However, it still retains two other advantages, namely:

1) It does not require a large linear operating range for both the optical source and receiver.

2) The signal contains strong timing information, which facilitates the timing extraction process at the receiver.

Thesis Objectives

There are two main objectives in this thesis:

1) To verify experimentally the validity of the amplitude theory regarding error mechanism in a 4-level PWM system.

2) To demonstrate experimentally that a self-generated clock recovery circuit in a 4-level PWM system can be easily implemented and that its BER performance is comparable to that of the same system being driven by a master clock.

To achieve these objectives, the following steps were taken:

1) A theoretical comparison was made between the slope theory and the amplitude theory.

2) In order to gain a better understanding of the error mechanism by experimental means, specific waveforms were transmitted and BER measurements taken, by sampling along different points of the signal waveform. These results were then compared with those calculated by the slope theory and the amplitude theory.

3) A monolithic PLL was used in the timing extraction circuit. This PLL system permits the easy adjustment of its parameters such as noise bandwidth, damping factor and loop gain.

4) Experimental measurements were made to obtain the sensitivity, or the range of variation of these parameter values, to the system BER performance.

5) Experimental measurements on system BER vs. optical power were carried out to verify that

a 4-level PWM optical fiber system, like its conventional coaxial system counterpart, requires a high gain, second-order PLL with small noise bandwidth and high damping factor. A PLL with such properties will generate a sufficiently stable clock to give a system BER performance with only a slight degradation as compared to that if driven by an almost ideal clock.

Thesis Organisation

This project was carried out in two stages, namely: 1)The investigation of error mechanisms and 2)Clock recovery using the PLL, in a 4-level PWM system. The next two chapters deal with the first stage, while Chapters 4, 5 and 6 concern the second stage of the project. Chapter 2 starts with an outline of a basic 4-level PWM optical fiber communication system to be followed by some analysis and comparison of the slope theory and the amplitude theory. Chapter 3 outlines the experimental 4-level PWM optical fiber communication system and the various experiments and results to demonstrate the general validity of the amplitude theory, as opposed to the slope theory.

Chapter 4 deals with timing extraction. It first discusses quantitatively the spectra of the various analog pulse modulation schemes, and qualitatively deduces the advantage of multi-level PWM over multi-level PAM and PPM with respect to timing information. It then defines the term timing jitter and further elaborates its meaning by discussing some of its major parameters. Chapter 4 concludes with a section comparing the pros and cons of using a tuned circuit and a PLL in a timing extraction process. Chapter 5 outlines some of the relevant basic principles of a PLL and discusses how the adjustment of its various parameter values can affect its performance in the timing extraction process. Chapter 6 briefly introduces the sources of clock jitter in an optical fiber communication system, particularly for a multi-level PWM system. Some basic principles of optimisation of a PLL are discussed and how these can be related to the situation when the PLL is employed in the timing extraction process. Various experiments were carried out to determine individually the sensitivity and the optimum value(s) of the various PLL parameters, such as noise bandwidth, damping factor and loop gain in relation to the BER performance of the system. It is found that these parameters can have a fairly wide range of variation in their values without greatly affecting the system BER performance. These results are not too surprising, given the strong timing information

contained in a multi-level PWM signal, and the use of the PLL, which is well suited to clock regeneration. The results demonstrate also that using a PLL in the timing extraction process gives good BER performance, which has only slight degradation as compared to that obtained when the receiver is timed using the original transmitter clock (master clock).

Chapter 2

ERROR MECHANISMS IN A MULTI-LEVEL PWM SYSTEM

Analog time modulation techniques such as pulse width modulation (PWM) and pulse position modulation (PPM) are known for their noise immunity. In Reference 17,18, it is shown that noise immunity improves with increasing slope of the received (PWM) pulse signal, as long as the system operates above its threshold level. This property of noise immunity has been extended to evaluate the Bit Error Rate(BER) for a quantized or multi-level PWM system, by a theory here referred to as "the slope theory" [1]. This theory relates the mean timing error to the slope of the pulse edges and to the noise variance at the 'slicing' level. However, as will be shown in this chapter, the timing error, known as "local" error[19] is typically not large enough to cause any significant error in a quantized PWM system. As in binary PCM systems, the main source of error here comes from what is known as "global" error[20]. Global errors, as characterised by another theory, here referred to as "the amplitude theory", are errors caused by noise superimposed on the signal 'ON' and signal 'OFF" levels. Therefore, the probability of error depends on the amplitudes of both the signal and of the noise, and on the 'slicing' level voltage. The computation of the BER in an optical fiber communication system is complicated by the presence of shot noise, which is not only signal dependent, but its statistical distribution is generally Poisson. Fortunately, this Poisson distrubution can be approximated with fairly good accuracy as Gaussian when the received optical power is sufficiently large. As the thermal noise of the system generally is Gaussian, the above approximation helps to ease the analysis of the error mechanism as well as the experimental measurements.

This chapter opens with the introduction of the operating principles of a 4-level PWM communication system. It then goes on to outline the sources of receiver noise, and presents the conditions under which the shot noise can be approximated as Gaussian. A discussion of the amplitude theory, including the evaluation of the BER for a 4-level PWM system, is given; this is followed by a brief outline of the slope theory. The chapter concludes with a comparison of the amplitude and slope theories and demonstrates that the slope theory is a particular case of the more general amplitude theory.

2.1 A 4-level PWM System

A model of a 4-level PWM optical fiber communication system is shown in Fig.2.1.

The encoder converts pairs of line bits from the binary signal source to single pulses of different widths according to the agorithm: 00 to t_0, 01 to t_1, 11 to t_2 and 10 to t_3 where, $t_0 < t_1 < t_2 < t_3$ (see Fig.2.2). This agorithm is based on the principle of Gray coding, whose advantages will be described in the next chapter. The encoded pulses, after gaining sufficient amplification drive the optical source.

In the receiver front end, the optical signals are converted back to electrical signals by the Avalanche photodetector(APD). When the front-end noise is dominated by preamplifier thermal noise rather than photodetector shot noise, the use of an APD can aid in increasing the sensitivity of the receiver[13].

The slicer determines the 'slicing' voltage level of the received PWM signal after the filter, and the waveform regenerator reproduces the pulse widths as modified by the system noise.

At the decision circuits, the various pulse widths are decoded into the corresponding binary pair sequence. The various widths are distinguished by 3 decision thresholds or samplers (τ_1, τ_2, τ_3) as illustrated in Fig.2.3, for a given time slot.

2.2 Sources of Receiver Noise

Stochastic noise refers to those random fluctuations that are inherently generated in any electronic component or circuit, over which the designer has no direct control. These fluctuation are superimposed on, and if large enough, can mask or distort any signals that are being processed in the circuit.

Fig.2.4 illustrates the major sources of noise associated with the detection and amplification processes in an optical receiver employing direct detection.

The quantum noise, dark current noise and surface leakage noise of photo-detector are all manifestations of shot noise, which is characterised by the Poisson statistical distribution. The dark current noise and surface leakage noise of commercially available detectors can be neglected as they are small compared with the thermal noise of the preamplifier. Quantum noise, generated from the photo-detection process, is fundamental in nature and sets the ultimate limit to receiver sensitivity. Normally, when a photodetector has no internal gain (that

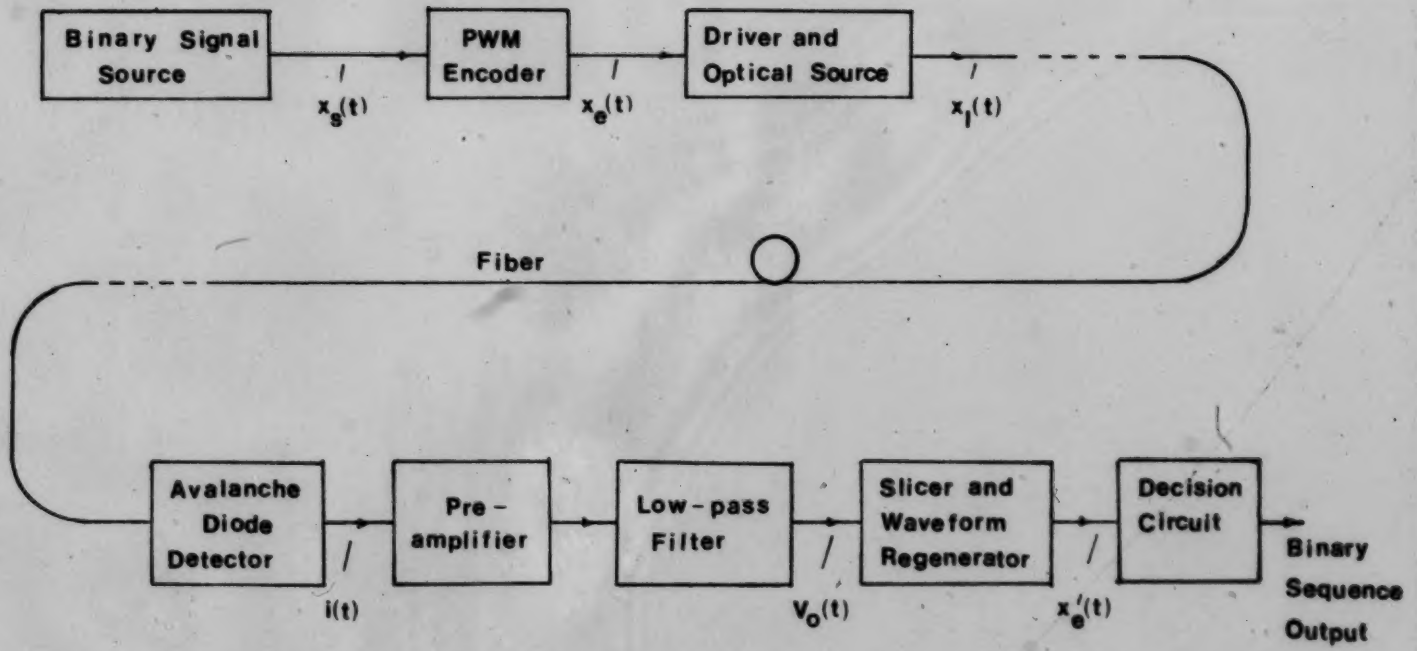


FIG. 2.1: BLOCK DIAGRAM OF A 4-LEVEL PWM OPTICAL FIBER COMMUNICATION SYSTEM

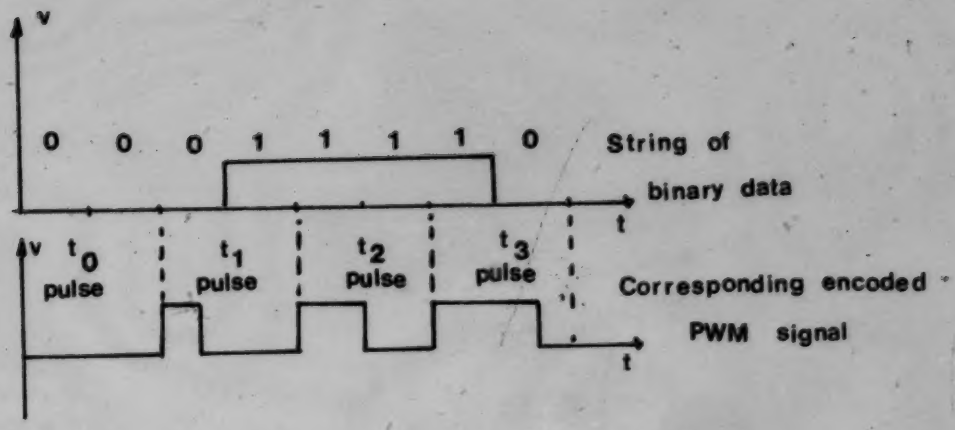


FIG. 2.2: ENCODING BINARY DATA TO A 4-LEVEL PWM SIGNAL

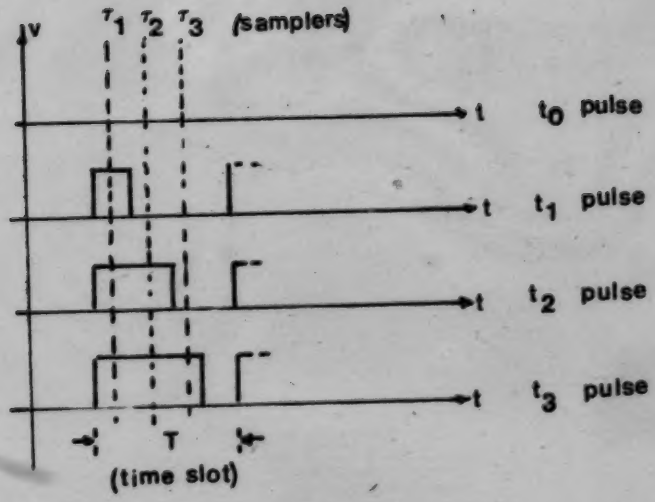


FIG. 2.3: DECODING A 4-LEVEL PWM SIGNAL

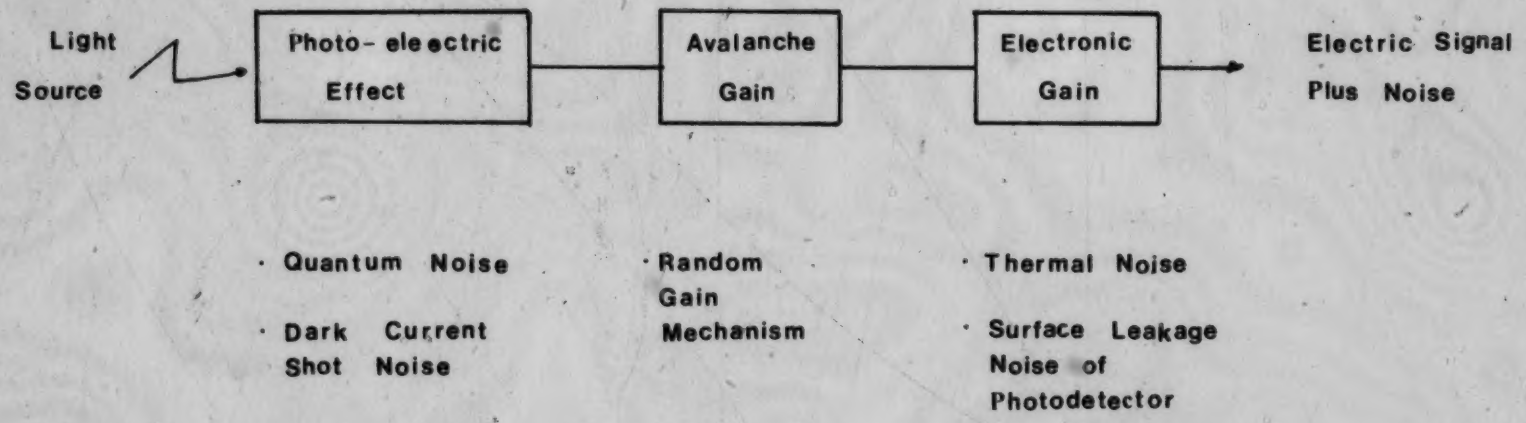


FIG. 2·4: NOISE SOURCES AT THE FRONT END OF AN OPTICAL RECEIVER

is , a PIN photodetector), then the thermal noise of the electronic amplifier dominates. When an avalanche photodetector is used (that is, one with internal gain), the relative significance of thermal noise is reduced. Unfortunately, this internal gain is a random process which, itself, introduces excess noise into the receiver. The excess noise is manifested by increased shot noise, above the level that results from amplifying the primary shot noise. In spite of this excess noise, a certain amount of avalanche gain can improve the sensitivity of optical receivers, which would otherwise be limited only by the thermal noise of the amplifier.

2.2.1 Shot Noise

From Personick[21], the average number of electrons created per second, a(t) is proportional to the intensity of the incident light,

$$a(t) = \frac{p(t)\eta}{hf} + n_0 \qquad (2.1)$$

where $p(t)$ is the light intensity or power in watts,

η is the photodetector quantum efficiency,

hf is the energy in a photon,

and n_0 is the dark current counts per second.

Equation (2.1) gives the average rate at which electrons are generated. The effect of n_0 is normally negligible when added to the thermal noise of the preamplifier, and hence is usually neglected.

For a given interval of time T, the probability that exactly N electrons are produced is given by

$$P\{N,\ (t_o,\ t_o + T)\} = \frac{\Lambda^N e^{-\Lambda}}{N!} \qquad (2.2a)$$

$$\text{where } \Lambda = \int_{t_o}^{t_o+T} n(t)dt \qquad (2.2b)$$

For this p.d.f. it can be shown that both the mean and variance are equal to Λ .

With avalanche gain, each primary electron can produce a number of secondary electrons. To take into account the excess noise introduced by the random nature of the

avalanche gain, this can be modelled by an equivalent amplifier with a gain M and a noise figure F_M . The mean square current fluctuation due to quantum noise at the output of an avalanche photodetector is given by[22],

$$\overline{i_q^2} = 2ei(t)M^2F_MB \qquad (2.3)$$

where e is the electron charge, i(t) is the signal current due to primary electrons and B is the system bandwidth.

2.2.2 Thermal Noise

Any dissipative element in a system introduces noise. Thus in an electronic circuit, any resistance results in thermal or Johnson noise as a consequence of the random thermal motions of the charge carriers. These are reflected as current fluctuations in the resistive component or as the corresponding voltage fluctuations across its terminals. The thermal noise due to the load resistance R is given by

$$\overline{i_n^2} = \frac{4KTB}{R} \qquad (2.4)$$

where K is Boltzmann's constant and T is the component temperature.

Hence R should be large to prevent excessive thermal noise. However, R is normally the input impedance of the preamplifier and higher R would mean smaller receiver bandwidth. To resolve this dilemma, a transimpedance amplifier is often used. A simplified schematic of a transimpedance amplifier is shown in Fig.2.5.

It may be shown that[23]

$$Bandwidth \quad B = \frac{A}{2\pi R_f C} \qquad (2.5)$$

and the thermal noise due to the feedback resistor R_f is given by

$$\overline{i_{th}^2} = \frac{4KTB}{R_f} \qquad (2.6)$$

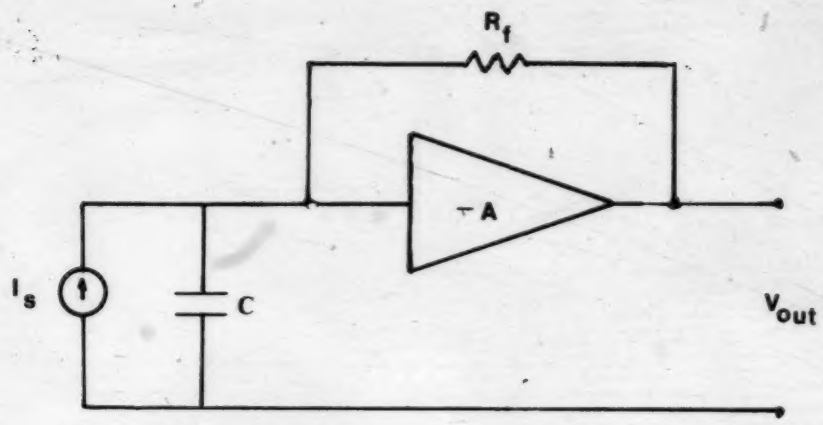


FIG. 2.5: TRANSIMPEDANCE AMPLIFIER

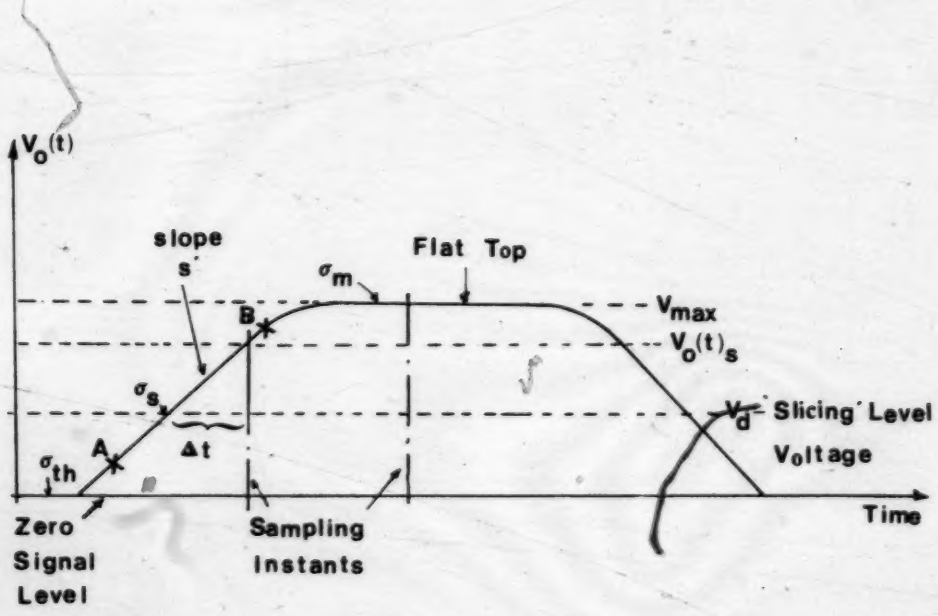


FIG. 2.6: NOISE VARIANCE CHANGES WITH SIGNAL LEVEL

Hence, the signal-to-noise ratio of the circuit can be improved by limiting the thermal noise through the use of large feedback resistor. This, however, will also reduce the receiver bandwidth but, as given by (2.5), this reduction can be offset by increasing the gain A.

The limit to the value of R_f will be the requirement of the amplifier dynamic range given by

$$V_{out} = I_{in} R_f \qquad (2.7)$$

The main problem with this amplifier, is one of amplifier stability. The use of a long feedback path around a high-gain, high-input impedance amplifier makes the circuit prone to high-frequency oscillations as a result of positive feedback via parasitic capacitance.

2.2.3 The Gaussian Approximation

In a digital communication system, if the sample value of the output signal $V_0(t)_s$ exceeds some threshold (the 'slicing' level) $a_k=1$ will be decided, otherwise a_k will be set equal to '0'. The probability of error is the probability that due to noise, $V_0(t)_s$ exceeds the 'slicing' level when a_k should be 0, or else $V_0(t)_s$ is below the 'slicing' level when a_k should be 1, for a given slot interval. In a receiver using an avalanche gain photodetector, calculation of the exact error probability is made difficult by the presence of randomly multiplied shot noise that is neither stationary nor independent of the data message. Various approximate techniques have been developed[24]. The technique which requires the least computation, yet for most practical purposes gives a fairly accurate result, is the well known Gaussian approximation method[25].

In the Gaussian approximation method, it is assumed that the sum of the thermal and shot noise is a Gaussian random variable. With this approximation, only the mean and variance of the noise need be known.

According to Webb[14], the multiplied shot noise can be approximated as a Gaussian random distribution, provided that

$$\frac{\Lambda}{F_M} \gg 1 \qquad (2.8)$$

where Λ is the average number of electrons per time interval T(see (2.2)), and

$$F_M = \{kM + (2 - 1/M)(1 - k)\} \qquad (2.9)$$

where k is the carrier ionisation ratio and M is the mean avalanche gain.

In the multi-level PWM system used in this project, an APD is used as the photodetector. Assuming that the photodiode dark current is small, then the shot noise is proportional to the signal current(or voltage after the transimpedance amplifier), and the overall noise variance, σ_T^2 will be linearly dependent on the signal amplitude. Hence with reference to Fig.2.6, the noise variance at any particular signal level $V_0(t)_s$, will be

$$\sigma_T^2 = \sigma_{th}^2 + (\sigma_m^2 - \sigma_{th}^2)\, V_0(t)_s / V_{max} \qquad (2.10)$$

where σ_m^2 is the noise variance at the maximum signal level and σ_{th}^2 is the noise variance at the zero signal level, which is normally dominated by the thermal noise of the preamplifier.

2.3 Error Mechanisms

Analysis of the error mechanisms as well as the error probability have been carried out using the slope theory[15]. However, this theory did not consider two factors; namely that:

1) the noise variance in an optical fiber receiver varies with the signal level. The slope theory only considers noise variance at the 'slicing' level and assumes this noise level to be the same for other parts of the signal waveform, even though they are at different signal levels.

2) in general, except for small pulses, the PWM waveforms have flat tops and the decision sampling instants could occur during these flat parts of the waveform rather than on the sloping part of the waveform (see Fig.2.6).

The amplitude theory suggests that the error probability depends on both signal and noise amplitude at the sampling instant.

In the following sections, both theories are discussed. The amplitude theory is shown to be the more generally applicable theory for analysing the error mechanisms in a PWM system, while the slope theory is a particular case of the amplitude theory which applies well to the analog case, but only under certain operating conditions to the quantized case.

2.3.1 The Amplitude Theory

The amplitude theory, attributes the BER of a multi-level PWM system to the amplitude of the signal and the amplitude of the noise superimposed on the signal 'ON' and signal 'OFF' levels. This type of error is known as global error.

The error mechanisms as described by the amplitude theory can be explained with the aid of Fig 2.6. There are two ways in which an error may occur. At a sampling time when the signal should be high, the noise amplitude may be large enough to lower the signal level below the 'slicing' level. At a time when the signal is 'OFF', the thermal noise of the preamplifier (assuming negligible dark-current noise), may cause a '1' to be detected. In all cases, the probability of error is given by

$$P(\sigma_{noise}) > \left| V_0(t)_s - V_d \right| \qquad (2.11)$$

where V_d is the 'slicing' level voltage, and $V_0(t)_s$ is the signal level at the sampling instant.

Using the Gaussian approximation method, we can assume that the noise variance at the different signal levels is Gaussian in distribution. Hence,

$$P_e = \int_X^\infty \frac{1}{\sqrt{2\pi}} e^{(-x^2/2)} dx \qquad (2.12a)$$

$$where,\ X = \left| \frac{V_0(t)_s - V_d}{\sigma_T} \right| . \qquad (2.12b)$$

and σ_T is the square root noise variance at signal level $V_0(t)_s$, and is given by (2.10). This leads to different values of P_e, depending on the time of sampling. For example, if we sample on the rising edge of the pulse, between point A and B, of Fig.2.6, then

$$X = \frac{(V_0(t)_s - V_d)}{\sigma_T}$$

may be related to the slope of the rising edge. That is, provided that the slope of the pulse edge

is linear, then

$$X = \frac{s'\Delta t}{\sigma_T} \qquad (2.13)$$

and, if the sampling instant is along the top of the pulse,

$$X = \frac{(V_{max} - V_d)}{\sigma_T} \qquad (2.14)$$

Generally, in an optical communication system, σ_T will be different at different sampling times, as given by (2.10), since it depends on the signal level at the instant of sampling. Fig.2.7 illustrates how errors can occur for each of the four cases of a 4-level PWM system.

It can be seen that an error occurs when either the noise is sufficient to lower the detected voltage in the case of a '1', or increase the voltage when a '0' should occur. For t_0 and t_3 pulses, only one of these can occur, but for t_1 and t_2, both are possible.

Hence, for a 4-level PWM signal, the probability of error is given by:

$$\begin{aligned} P(\varepsilon) = 1 &- P_0(\textit{probability of receiving } t_0 \textit{ if } t_0 \textit{ is transmitted}) \\ &- P_1(\textit{probability of receiving } t_1 \textit{ if } t_1 \textit{ is transmitted}) \\ &- P_2(\textit{probability of receiving } t_2 \textit{ if } t_2 \textit{ is transmitted}) \\ &- P_3(\textit{probability of receiving } t_3 \textit{ if } t_3 \textit{ is transmitted}) \end{aligned}$$

Referring to Fig.2.7,

$$\begin{aligned} P(\varepsilon) = 1 &- P_0(P(0/0))^3 - P_1\{(P(0/0))^2 P(1/1)\} \\ &- P_2\{P(0/0)(P(1/1))^2\} - P_3(P(1/1))^3 \end{aligned} \qquad (2.15)$$

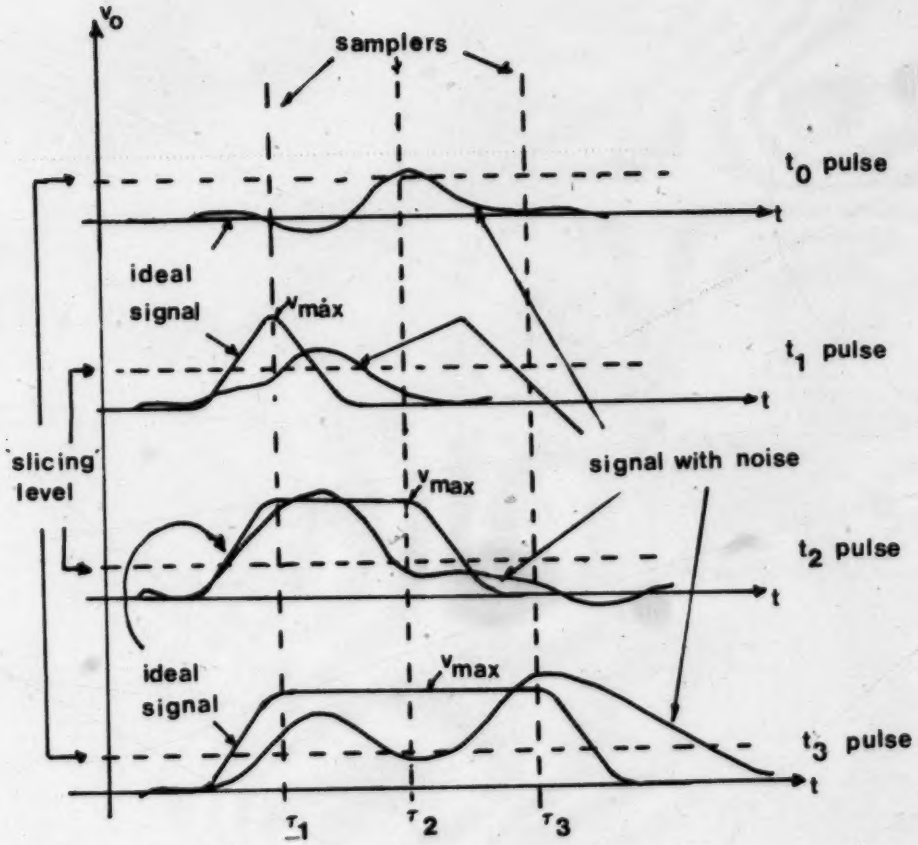


FIG. 2.7: 4-LEVEL PWM SIGNALS WITH NOISE

where P_j is the probability of sending t_j pulse,

P(0/0) is the probability of receiving a signal low when signal low is transmitted and,

P(1/1) is the probability of receiving a signal high when signal high is transmitted.

Equation (2.15) is derived on the assumptions that,

1) there is no error correction code in the decoder,

2) all the maximum amplitudes of the signal for t_1,t_2 and t_3 pulses are equal,

3) all sampling instants are taken at the maximum amplitude of the signal, and

4) there is negligible intersymbol interference (I.S.I.).

P(0/0) and P(1/1) are given by

$$P(0/0) = \int_{-\infty}^{\frac{V_d}{\sigma_{th}}} \frac{1}{\sqrt{2\pi}} e^{(-x^2/2)} dx \qquad (2.16)$$

$$P(1/1) = \int_{-\infty}^{\left|\frac{V_{max}-V_d}{\sigma_T}\right|} \frac{1}{\sqrt{2\pi}} e^{(-x^2/2)} dx \qquad (2.17)$$

If the transmitted PWM signals are truly random, then P_j of (2.15) will be all equal to 1/4.

Equations (2.16) and (2.17) indicate that the 'slicing' voltage level does play a part in influencing the overall probability of error $P(\epsilon)$. Since P(0/0) and P(1/1) have equal weight in (2.15), the optimum position for the 'slicing' level voltage is when

$$P(0/0) = P(1/1) \qquad (2.18)$$

It is to be noted that lowering the system bandwidth on the one hand helps to restrict the noise level but, on the other hand, causes an increase in the rise- and fall times of pulse edges. If too small a system bandwidth is used this will give rise to a significant reduction in the amplitude of the PWM pulses, particularly that of the smaller pulse t_1, as well as possible I.S.I. effects, and hence a smaller SNR(signal-to-noise ratio). Thus, a compromise must be

established in the system bandwidth to restict the values of noise level as much as possible while at the same time not sacrificing too much in terms of the maximum magnitude and waveform integrity of the pulses.

2.3.2 The Slope Theory

Using the above theory, the BER is determined by relating the mean timing error to the slope of the pulse edges and the noise variance at the 'slicing' level. This is illustrated in Fig.2.8.

The relationship between the timing error, $\Delta\tau$, called the local error, and n_t , the instantaneous noise amplitude is given by

$$\frac{n_t}{\Delta\tau} = \left|\frac{dV_0(t)}{dt}\right|_{t_s} \tag{2.19}$$

According to the slope theory, to minimise the effect of n_t on $\Delta\tau$, the 'slicing' level V_d is chosen at the point of maximum slope. To normalise the noise,

$$Let\ X = \frac{n_t}{\sigma_s} \tag{2.20}$$

where σ_s is the standard deviation of the noise at the 'slicing' voltage level.

From (2.10) and (2.19),

$$X = \frac{n_t}{\sigma_s} = \left|\frac{dV_0(t)}{dt}\right| \frac{\Delta\tau}{\sigma_s} \tag{2.21}$$

$$= S\Delta\tau \tag{2.22a}$$

$$where\ S = \left|\frac{dV_0(t)}{dt}\right| \frac{1}{\sigma_s} \tag{2.22b}$$

Using the Gaussian approximation method, where σ_s can be assumed to be Gaussian in distribution; therefore,

$$P(S) = \frac{1}{\sqrt{2\pi}} exp(-S^2/2) \tag{2.23}$$

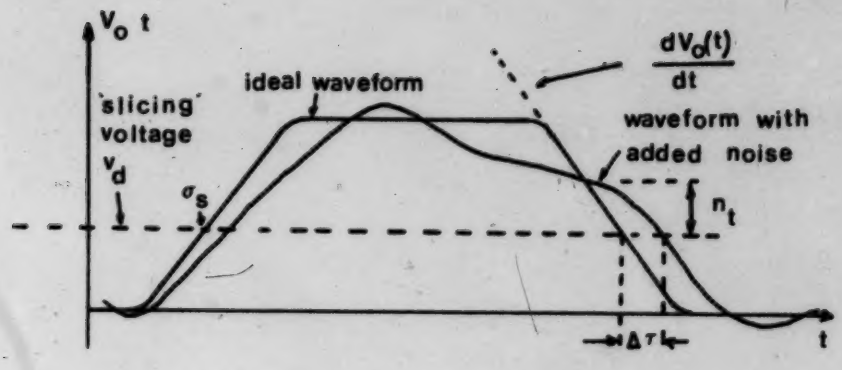


FIG. 2.8: EFFECT OF SLOPE AND NOISE ON TIMING ERROR

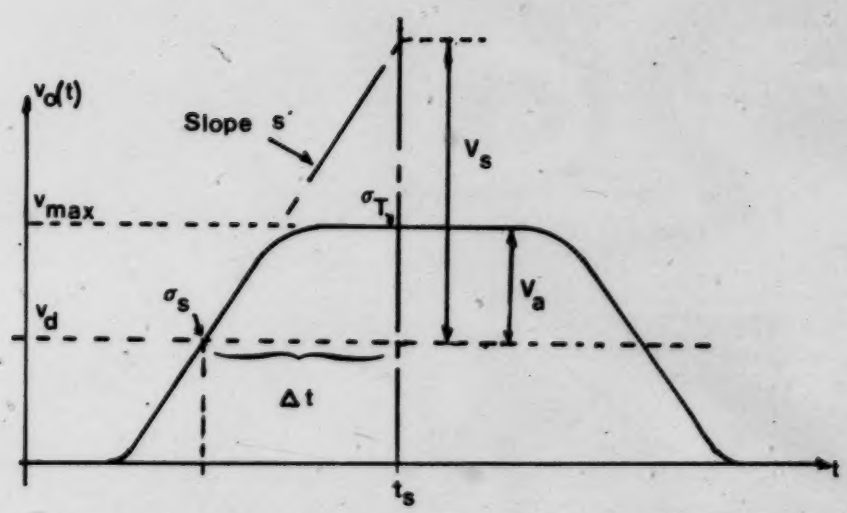


FIG. 2.9: WAVEFORM COMPARING SLOPE THEORY AND AMPLITUDE THEORY

A detailed evaluation of the system BER can be found in the Reference 1. In summary, the slope theory deduced that, for a given received power, the BER is reduced by increasing the bandwidth. Also, to minimise the noise effect on the received pulse width, the 'slicing' level should be at the point of maximum slope.

2.3.3 Slope Theory: A Particular Case of the Amplitude Theory

This section shows that the slope theory, under certain operating conditions, is basically an extended version of the amplitude theory.

Assume that the detected output waveform is as illustrated in Fig.2.9 and that the noise variance remains constant for all signal levels.

From the slope theory, the probability of receiving a low at a sampling time Δt is (see Fig.2.9),

$$P_{e_s} = \int_{\Delta t}^{\infty} \frac{S}{\sqrt{2\pi}} \exp(S^2\tau^2/2)d\tau \qquad (2.24)$$

$$P_{e_s} = \int_{S\Delta t}^{\infty} \frac{1}{\sqrt{2\pi}} \exp(\tau^2/2)d\tau \qquad (2.25)$$

For the amplitude theory, the probability is

$$P_{e_a} = \int_{\frac{V_a}{\sigma_T}}^{\infty} \frac{1}{\sqrt{2\pi}} \exp(x^2/2)dx \qquad (2.26)$$

Equations (2.25) and (2.26) are integrations of a standard normalised Gaussian function, the difference being in their integration limits.

From (2.22b) and referring to Fig.2.9,

$$S\Delta t = \frac{s'\Delta t}{\sigma_s} = \frac{V_s}{\sigma_s} \qquad (2.27)$$

We have assumed that $\sigma_T = \sigma_s$, therefore,

$$\frac{V_s}{\sigma_s} > \frac{V_a}{\sigma_T} \qquad (2.28)$$

which implies that

$$P_{e_a} > P_{e_s} \qquad (2.29)$$

and this inequality is even greater if $\sigma_T > \sigma_s$, as usually is the case in optical fiber communication system.

In summary, for very small Δt , that is, when the sampling instant happens to fall on the linear part of the pulse sloping edge, P_{e_s} which is caused by local errors will be equal to P_{e_a} , provided $\sigma_T = \sigma_s$, or approximately equal, if σ_T is only marginally greater than σ_s . Under these conditions, both theories will converge to the same results. In other words, the general amplitude theory converts to the slope theory via the fact that the amplitude, V_a of (2.26) is given by the product of s' and Δt . However, as Δt becomes larger and for a non-linear pulse edge (that is the slope changes with signal level), and the possibility of a flat-top pulse (Fig.2.9), the product of s' and Δt will no longer be a good approximation to the amplitude. This is illustrated by V_a and V_s in Fig.2.9. Hence, in general as Δt becomes large, and for a flat-top pulse, the slope theory tends to underestimate the BER. As two out of the 4-PWM signal pulses have flat tops, and the decision thresholds or sampling instants occur on these flat tops, the slope theory will give a significant error in the computation of the BER; that is, it will underestimate it. In addition, for large signal amplitude, the difference between σ_T and σ_s generally will become

significant. This further increases the underestimation of the BER.

In the next chapter, an experimental investigation of the error rate in a PWM system is described. The results agree well with the amplitude theory.

Chapter 3

EXPERIMENTAL INVESTIGATION OF ERROR MECHANISMS

The way in which errors occur in a multi-level PWM system has been discussed in the last chapter.

A 4-level PWM system was original built by Mr. Dai Xianda to study the feasibility of PWM and also to verify the slope theory. Though the whole system was successfully built, the experiment was not completed due to lack of time. Hence, one of the objectives of the work described in this thesis was to continue the experiment on the investigation of error mechanisms in a 4-level PWM system. Some minor modifications were made to the system, namely:

1)a better APD photodetector and preamplifier, which was designed and built by Mr. Colin Kelly, was used (refer to his thesis[26]).

2)A d.c. level shifter was added to the detector circuit to allow adjustment of the 'slicing' voltage level. This feature was used in some of the experimental tests.

3)Some of the delay elements (NAND gates) in the decision circuit, were replaced by a pair of monostables. This method of delay using monostables allows more flexibility in the adjustment of the delay.

In addition to the above modification, a clock recovery circuit was added in the receiver section, although this was not used in the experiments that will be discussed in this chapter.

3.1 The Overall Experimental 4-level PWM System

Fig.3.1 illustrates the overall experimental 4-level PWM system. The Data Analyser was used both as a binary signal source as well as an error detector.

3.1.1 The Transmitter

The main fuctions of the transmitter circuitry are

1)Conversion of binary codes into their respective 4-level pulse width coding.

2)Conversion of the electrical PWM signal to an optical signal, with adjustable optical power output at wavelength 830nm for compatibility with the optical fiber. Fig.3.2 illustrates the schematic diagram of the transmitter. IC1 splits the line code into two parallel streams of identical data with one stream delayed by one clock cycle with respect to the other. IC4, IC5

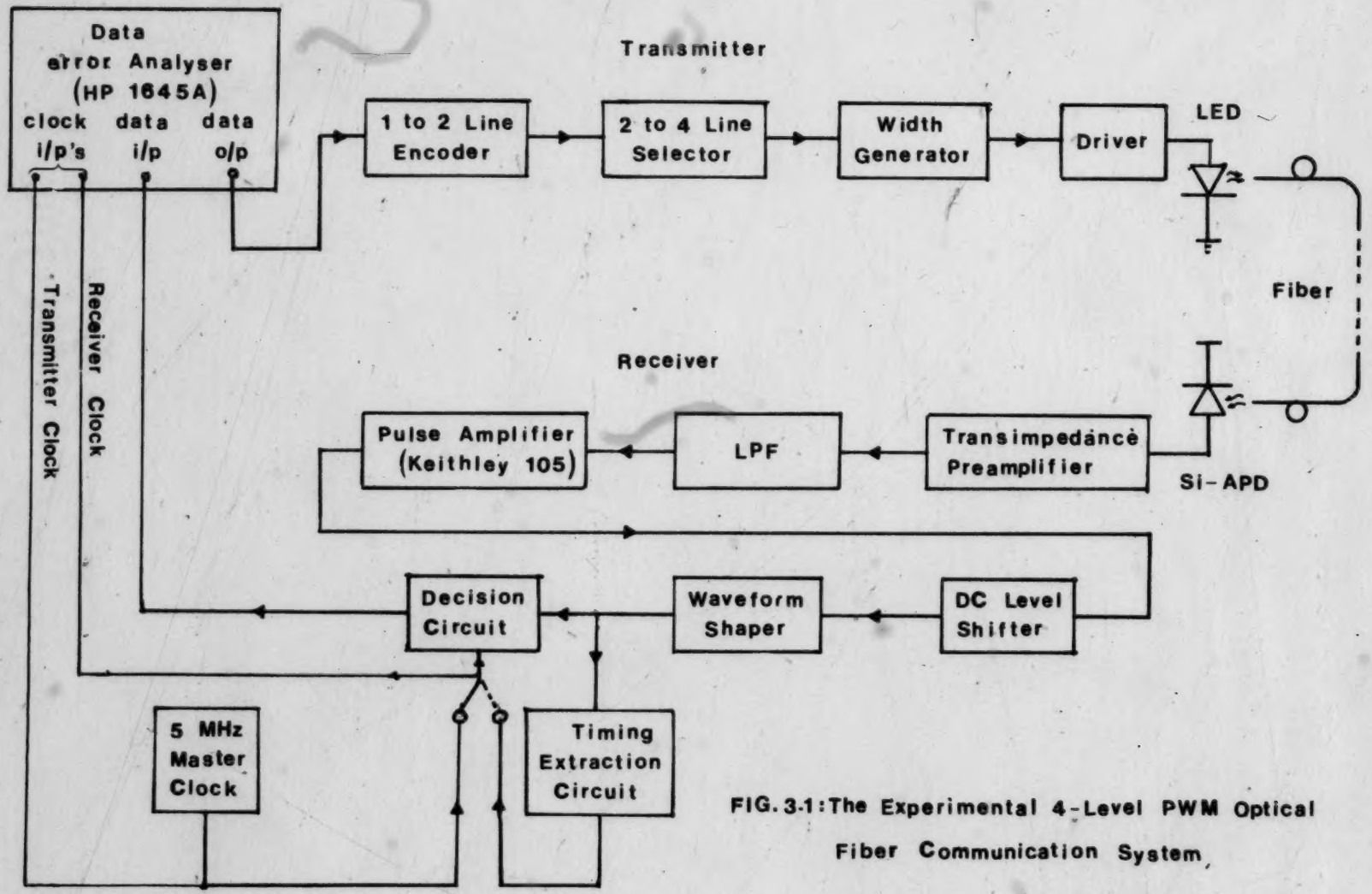


FIG. 3.1: The Experimental 4-Level PWM Optical Fiber Communication System

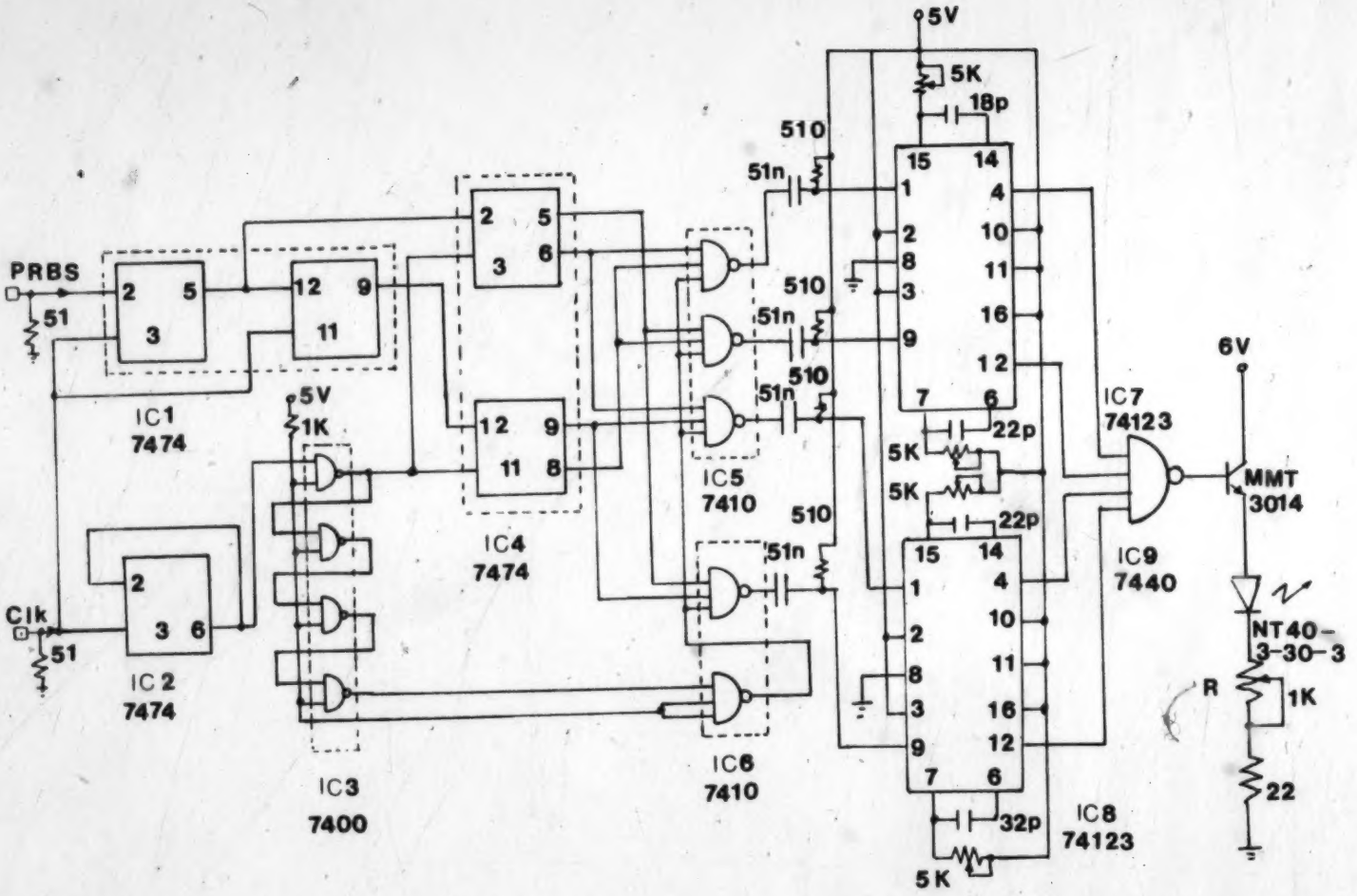


FIG. 3.2: THE TRANSMITTER FOR THE 4-LEVEL PWM OPTICAL FIBER COMMUNICATION SYSTEM

and part of IC6 function as the 2 to 4 line selector, which triggers the following monostables IC7 and IC8, to produce pulses of different widths. The output of IC9 switches on the transistor MMT3014 and hence also the optical source for a time duration which depends on the width of the pulses. The variable resistor R, in series with the optical source, controls the LED current, and hence the optical source output intensity.

Gray coding[27] was used so that encoded PWM pulses of adjacent width differ by one binary digit. This helps to minimise probability of error upon reception, as the most likely error caused by noise involves the erroneous selection of an adjacent pulse width, hence giving only one binary bit error. Therefore the binary to width conversion agorithm is: 00 to t_0, 01 to t_1, 11 to t_2 and 10 to t_3 where t_0 is zero width, or no pulse, t_1 is 100ns, t_2 is 200ns and t_3 is 300ns in duration. The binary rate is 5Mbits/s which means that the transmitting rate for the 4-level PWM signal is 2.5M symbol/s or a time period of 400ns/symbol.

An LED #NT 40-3-30-3 (made by Northern Telecom Ltd.) was used as the optical source. It has a 3dB bandwidth of 44MHz, and an emission wavelength of 830nm and a FWHM spectral width of typically 40nm.

3.1.2 The Optical Fiber

A graded index fiber (Siecor Super Fat Fiber Cable #155) with bandwidth of 5MHz-Km was used. This fiber has an attenuation of 35 dB/Km at 830nm and a numerical aperture of 0.4. Though the characteristics of this fiber are far below the quality of presently available fiber in terms of bandwidth and attenuation, it is useful for laboratory work because it can simulate a long good quality fiber with just a short length of poor fiber. In this experiment, approximately 400m of the Super Fat fiber was used.

3.1.3 The Optical Receiver

The block diagram of the digital optical receiver is shown in Fig.3.1 and the detailed circuit is shown in Fig.3.3. There are two options for clock synchronisation of the receiver, namely:

1)Using an external master clock to drive both the transmitter and the receiver or

2)using a self regenerated clock, recovered from the PWM signal itself. Option (1) is used for the investigation of the error mechanism described in this chapter, as it is able to provide 'ideal'

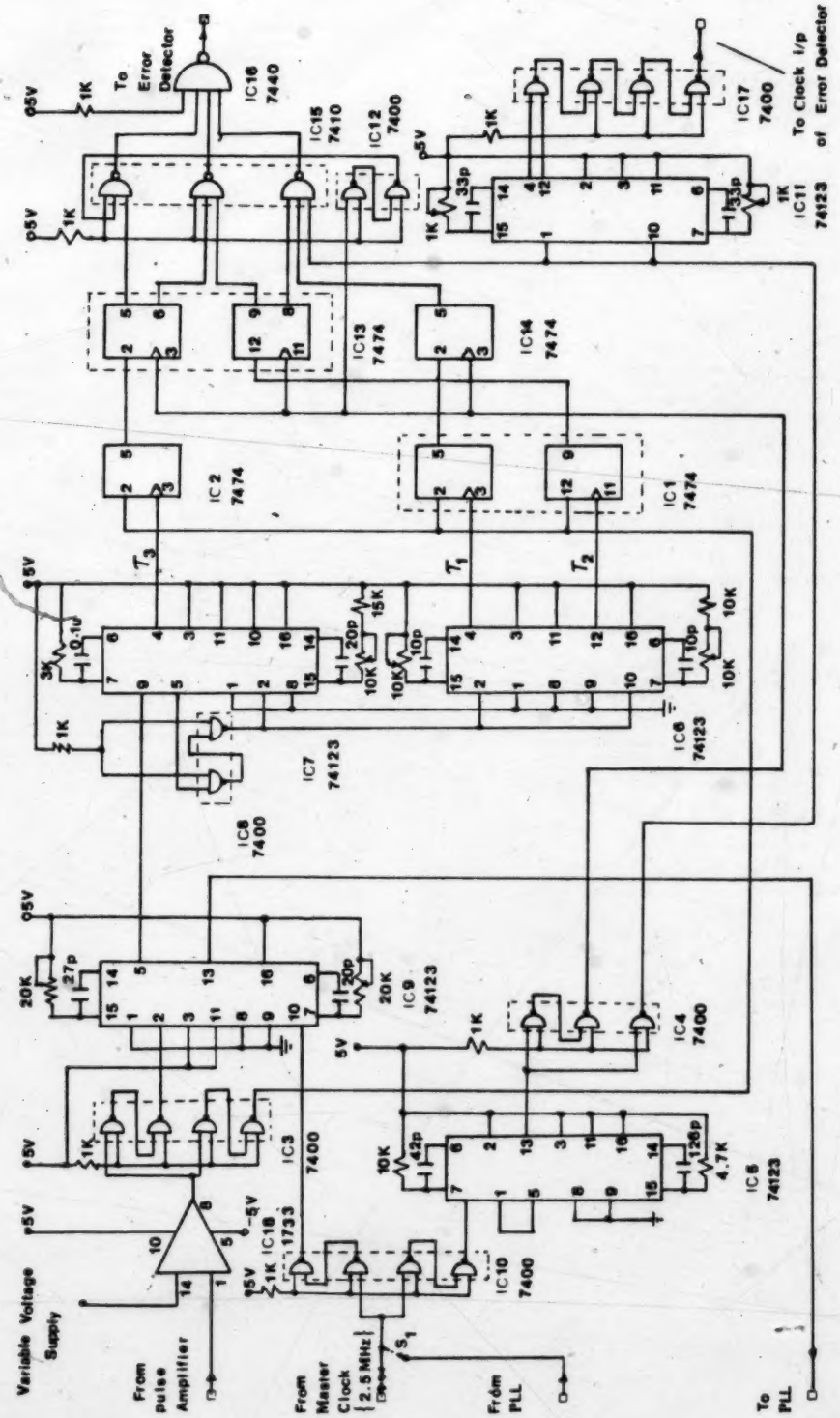


FIG.3.3: THE DECODER FOR THE 4-LEVEL PWM OPTICAL FIBER COMMUNICATION SYSTEM

clock timing for the receiver. This 'ideal' timing is required because some experiments require the position of the sampling instants (or the timing clock) to be adjusted with respect to the incoming PWM signals, and any significant instability (as there would be in a self-regenerated clock) would obscure the analysis of the measurement results. The design and use of option (2) will be discussed in the following three chapters.

An APD coupled to a transimpedance amplifier was used at the front end of the receiver; their advantages were discussed briefly in Chapter 2, and a more detailed discussion can be found in Reference 28,29. The detailed circuit diagram and design is given in C. Kelly's thesis[26]. The APD (C30908E made by RCA) has a quantum efficiency of 77% at 830nm, a mean gain of 150 and an ionization ration k=0.02. Hence, from (2.9), F_M is calculated to be equal to 4.953. At an average received optical power of 0.1nW, and at a symbol rate of 2.5 Mbit/sec, from (2.8),

$$\frac{\Lambda}{F_M} \approx 129 >> 1 \qquad (3.1)$$

Since all the experiments to be described were conducted with a received optical power much greater than 0.1 nW, the Gaussian approximation method can be used to give an accurate estimation of BER.

Following the APD and the preamplifier, a commercially available pulse amplifier(Keithley 105 Pulse Amplifier, with a voltage gain of 100 and bandwidth of 500MHz) was used to provide sufficient signal voltage to trigger the waveform regenerator(shaper). The d.c. shifter provides an easy adjustment of the 'slicing' voltage of the signal, as required in one of the experiments. As shown in Fig.3.3, the d.c. shifter is basically made up of a two input linear amplifier(1733), with one of its inputs connected to a variable d.c. voltage supply. Adjustment of this d.c. voltage controls the d.c. level of the PWM signal, and hence the 'slicing' voltage level.

At the decision logic circuit, pulses of different widths are applied to the inputs of the three positive edge-triggered flip-flops to enable their widths to be compared with the three decision threshold timing signals or samplers as depicted in Fig.3.4 and Fig.3.5. If during a given time slot or interval, the longest pulse (t_3 pulse) is received, inputs at A, B and C will all be set to the logic high state and the bit pair '10' will be produced at the output of the decision

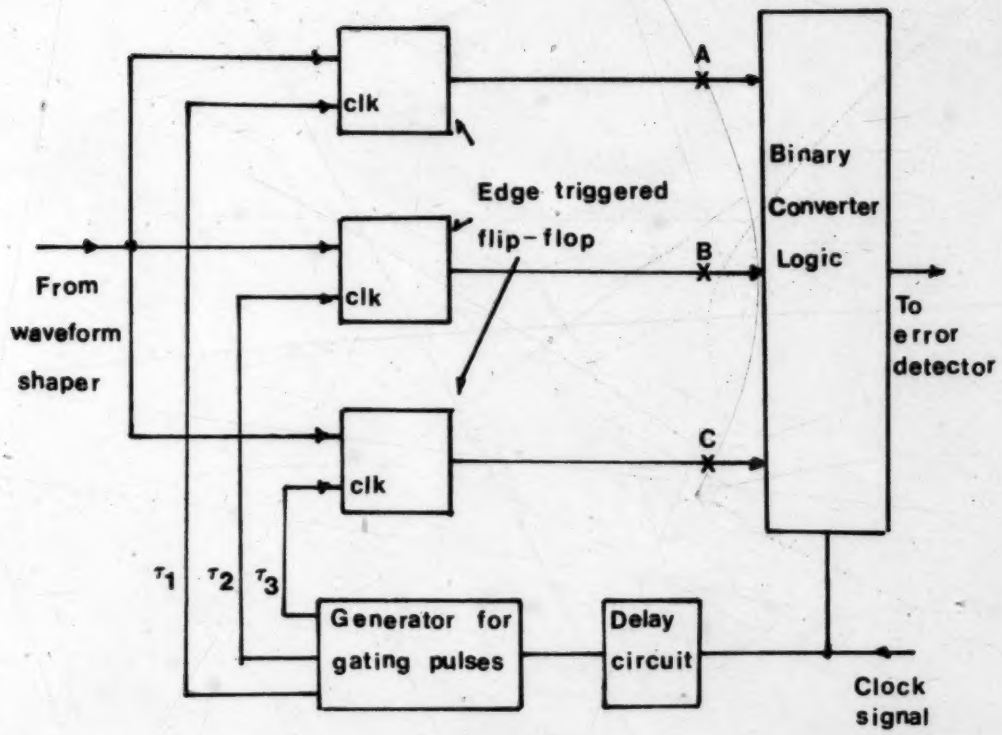


FIG. 3·4: THE DECISION LOGIC SCHEMATIC

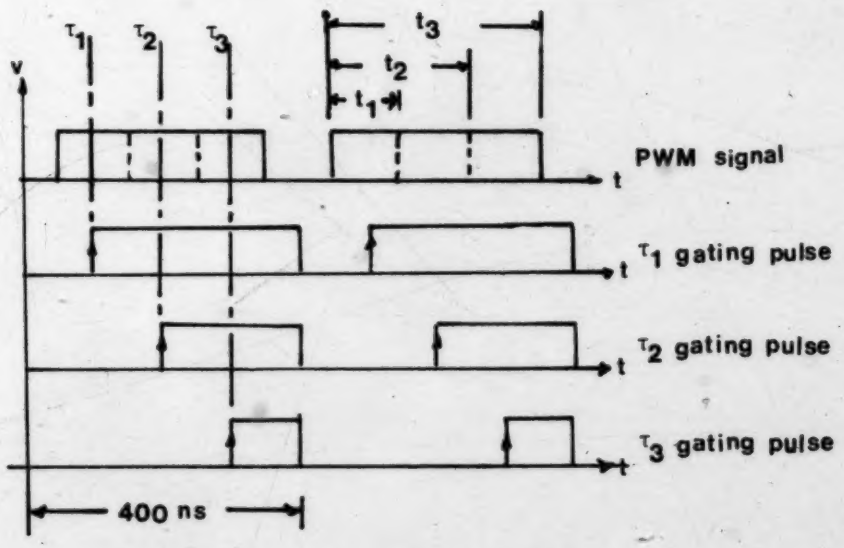


FIG. 3·5: TIMING DIAGRAM FOR THE GATING PULSES

logic circuit. For other pulses, the various combinations of the inputs A, B and C together with the decoded binary output are summarised in Fig.3.6.

The binary sequence produced by the decision logic is compared to the initially transmitted binary sequence using the Data Analyser to give the BER.

The delay circuit of Fig.3.4 was used to adjust the relative position of the decision thresholds or samplers with respect to the PWM signals.

3.2 Measurements and Results

In order to test the causes of error as discussed in the preceeding chapter, experiments were conducted using only the t_1 or t_3 pulses. For the short t_1 pulse, the error rate can be related to the pulse slopes (see (2.18)). whereas the t_3 pulse allows a check of the error due to amplitude, (independent of the slope, (2.23)). Further, to determine the cause of error, that is, which of the possible events could occur as in Fig.2.8, two of the three voltage samples were set low or high, so that the effect of noise at only one point in the waveform could be observed. The generation of the t_1 and t_3 pulses could be achieved since the continuous 101010.. bit stream can be clocked as a 01 sequence or as a 10 sequence. The receiver bandwidth was set to approximately 10MHz so as to give approximately triangular and trapezoidal waveforms for the t_1 and t_3 pulses, respectively.

3.2.1 BER as a Function of Time Delay

i) *For t_3 Pulse*

Using the 10 sequence a series of t_3 pulses was transmitted as shown in Fig.3.7. The samples at τ_1 and τ_2 were held at logic '1', so that the effect of noise at time τ_3 only could be observed. An error will be caused if the noise voltage causes the signal to dip below the threshold at the time τ_3. The 'slicing' level was set approximately at the centre of the received PWM waveform. The time Δt of τ_3 was now varied using the delay circuit of Fig.3.4, and the BER was measured. The results are shown in Fig.3.8.

Pulse Width	A B C	Decision Logic Output	
t_0	0 0 0	0 0	
t_1	1 0 0	0 1	Valid
t_2	1 1 0	1 1	code
t_3	1 1 1	1 0	
	0 0 1	1 0	
	0 1 0	1 1	Invalid
	0 1 1	1 0	code
	1 0 1	1 1	

FIG.3 6: DECODING THE PWM SIGNAL

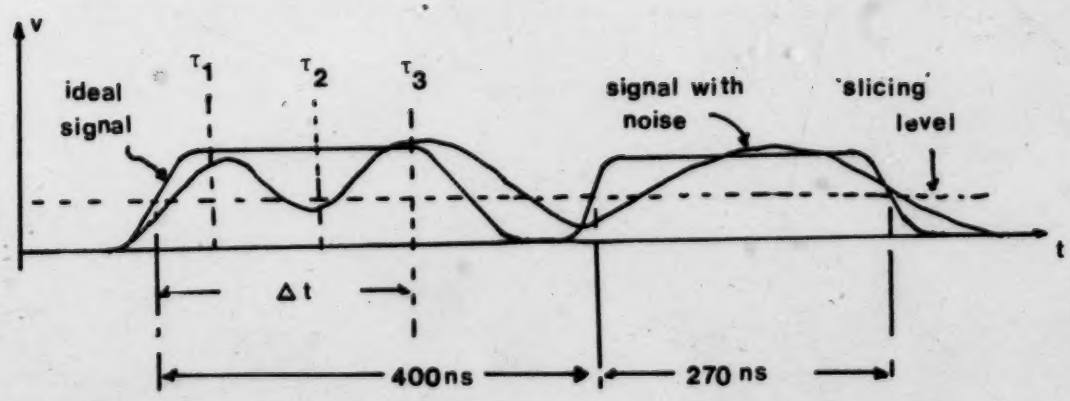


FIG.3.7: PWM WAVEFORM FOR A 10 PATTERN SEQUENCE

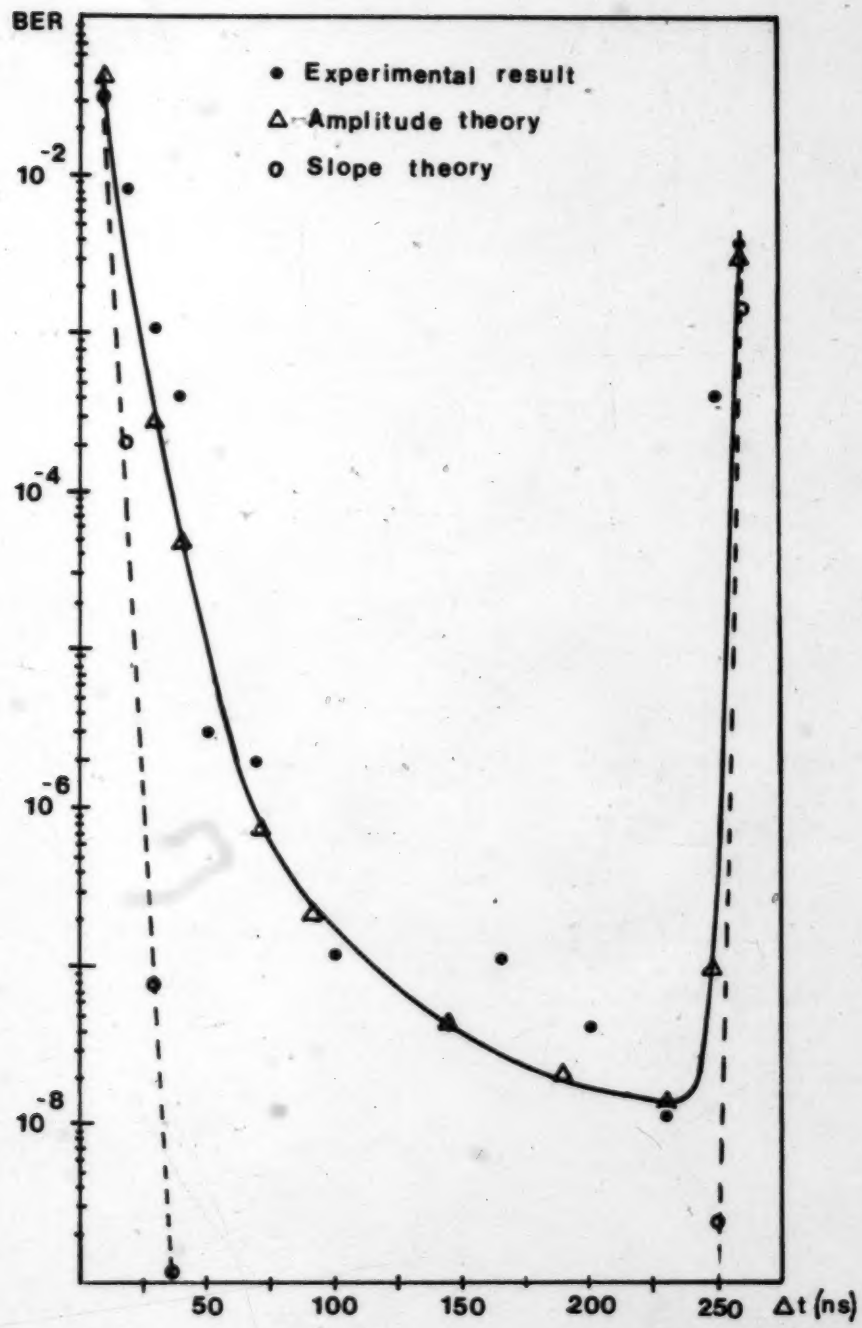


FIG. 3.8: BER AS A FUNCTION OF TIME DELAY (t_3 PULSE)

ii) *For t_1 Pulse*

A similar measurement was made sending the t_1 pulse, with τ_2 and τ_3 set to low('0'). There will be an error if the signal is below the 'slicing' level at the time τ_1. The BER measurement as a function of Δt for τ_1 is shown in Fig.3.9.

3.2.2 Effect of Varying the Slicing Voltage Level

For this test a 00000001 pattern (7:1) was generated and the 'slicing' voltage V_d was varied (Fig.3.10). The BER was recorded. The measurements were repeated for several different received signal amplitudes. The results are shown in Fig.3.11. In this test, for small V_d, the errors will be due to amplifier noise causing a '1' to be recorded at either τ_2 or τ_3. Conversely for large V_d, the error will be mainly due to noise causing the '1' at time τ_1 to be sampled as a '0'.

3.2.3 BER as a Function of Received Optical Power

In this test, a pseudo-ranom sequence of length $10^{20}-1$ was sent with the system fully operational. Results were taken for effective receiver bandwidths of approximately 5MHz and 10MHz. For the reduced bandwidth, unfortunately, the t_1 pulse height at the receiver was reduced as compared to the t_2 and t_3 pulses, due to the limited rise time of the receiver. The results are shown in Fig.3.12.

3.3 Discussion of Results

The experimental results given in section 3.2 generally agreed quite well with the theory given in Chapter 2. The theoretical points in Fig.3.8 were calculated from (2.17) where values of ($V_0(t)_s - V_d$) and σ_T were estimated from experimental observation. The theoretical points computed by the slope theory (see Fig.3.8) do not generally agree with the experimental results, and as discussed in Chapter 2, it tends to underestimate the BER. This underestimation is clearly shown in Fig.3.8, especially when the signal pulse starts to flatten. The other factor that was discussed is the changing noise variance with signal level in an optical fiber system. The results shown in Fig.3.8 illustrate that the BER computed by the slope theory along the almost linear pulse edge region (that is not the flattened top region of the pulse) is again an underestimation.

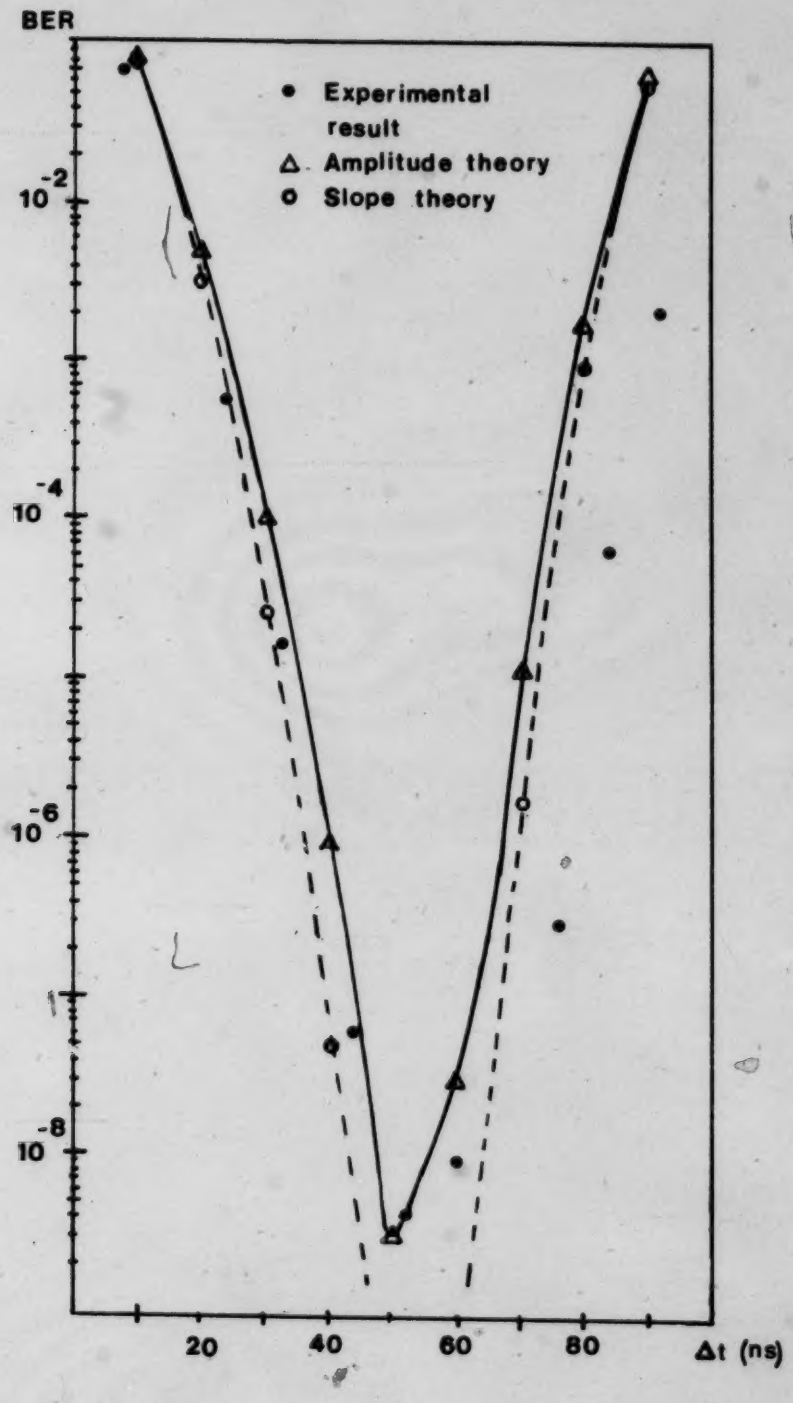


FIG.3.9: BER AS A FUNCTION OF TIME DELAY (t_1 PULSE)

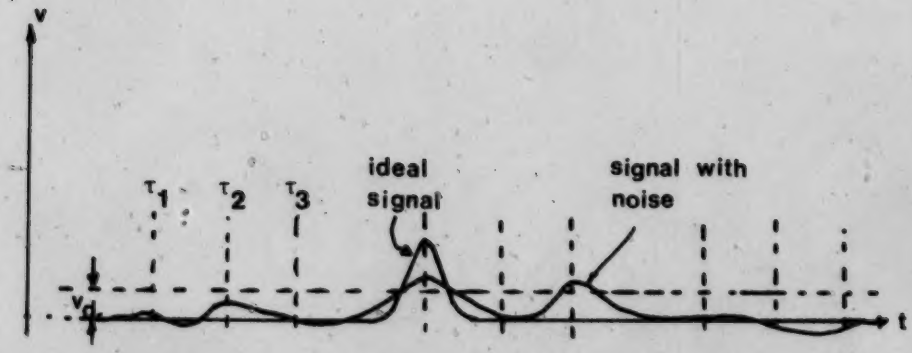


FIG.3-10: EFFECT OF NOISE ON BER AS A FUNCTION OF 'SLICING' VOLTAGE

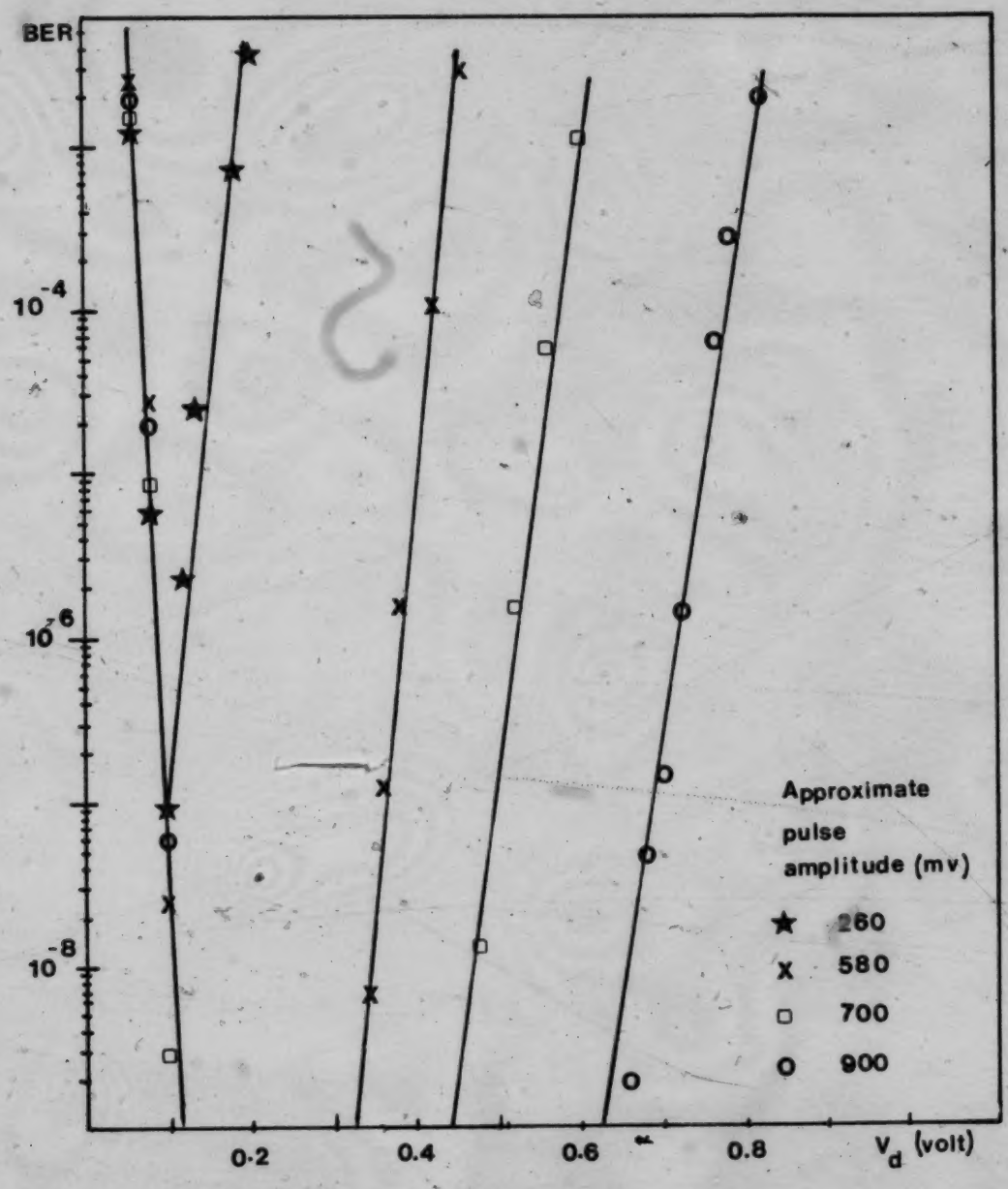


FIG. 3.11: CHANGE IN THE EFFECT OF NOISE ON BER AS THE SLICING LEVEL INCREASED FOR VARIOUS PULSE AMPLITUDES

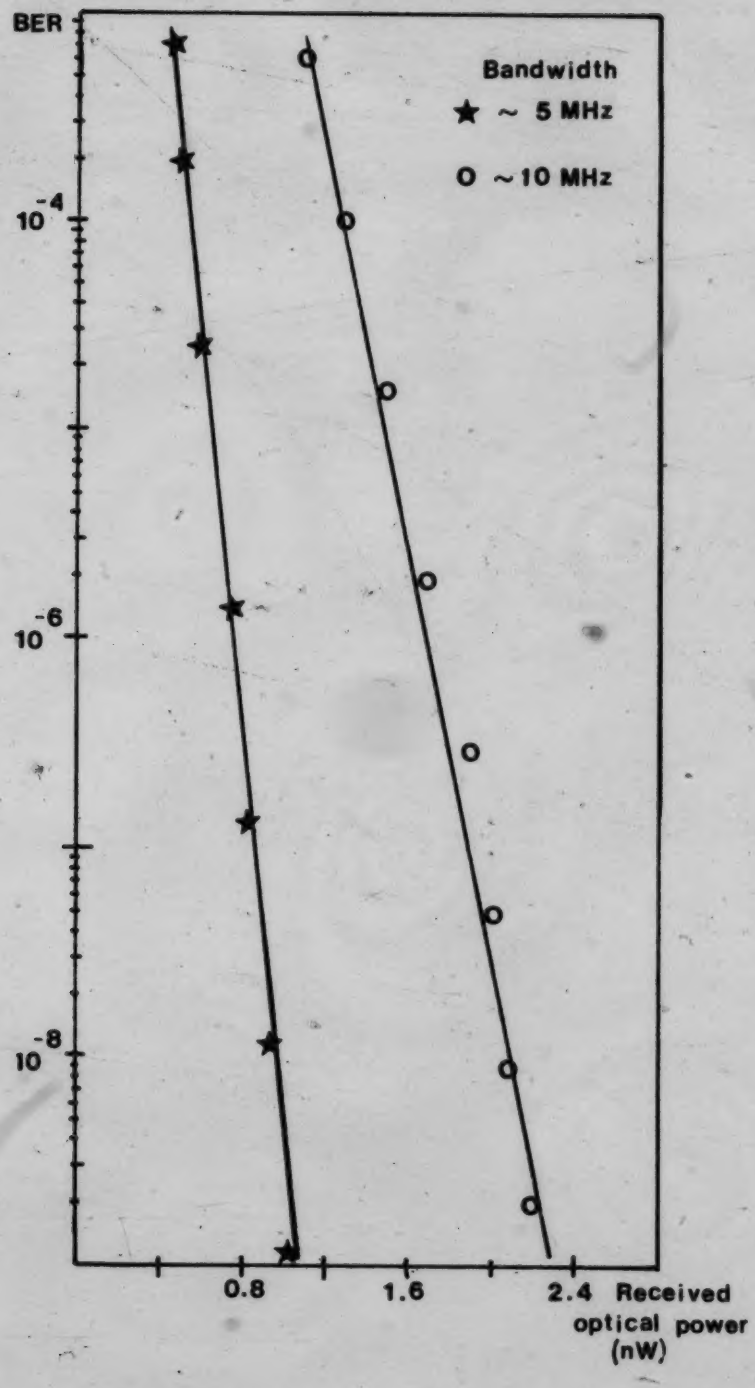


FIG.3.12: BER AS A FUNCTION OF RECEIVED OPTICAL POWER

The slope theory seems to fit better with the smaller pulse t_1, as shown in Fig.3.9. This could be explained by the fact that the amplitude of the pulse is small, hence the difference in noise variance along top and bottom of the signal is not significant. Secondly, and perhaps the more importantly, the t_1 pulse has fairly linear edges and only a very slight flattened top. In short, the slope theory could give a better estimation provided: 1)the slope at the sampling instant is approximately the same as the slope at the 'slicing' level and 2) that the noise variance along different signal level does not have a significant difference. The t_1 pulse in this experiment satisfies these two conditions.

The results shown in Fig.3.11 illustrate that the BER characteristic for low values of the 'slicing' voltage is fairly independent of the waveform amplitudes, and hence independent of the slope of the signal. It is the amplitude of the noise at the signal 'OFF' level that determines the BER characteristic.

Finally, the results in section 3.2.3 (see Fig.3.12) show that the system can give a BER of 10^{-9} with a received optical power of less than 1.2nW only if a proper channel bandwidth is chosen. A larger channel bandwidth might improve the rise and fall time of the pulse edges, but suffers in terms of SNR(signal-to-noise ratio), and hence BER performance. Conversely, there is also a bound on the lower limit to the channel bandwidth. As the bandwidth decreases, the rise and fall times of the received waveform increase, which causes reduced amplitude, particularly for the shortest pulse (t_1 pulse) as compared with t_2 and t_3 pulses. This again will effect the overall SNR, hence BER performance. In addition, further reduction in the bandwidth will inevitably lead to I.S.I.(intersymbol interference) effects. In short, there is an optimum bandwidth which restricts the level of noise, while causing only a slight impairment of the signal pulse amplitudes.

Chapter 4

TIMING EXTRACTION AND JITTER

4.1 Introduction

In baseband digital systems, the output of the receiver must be sampled at precise sampling instants in order to recover the original signal. To perform this sampling, a clock signal is needed at the receiver that is synchronised with the clock signal at the transmitter. Three general methods in which this synchronisation can be obtained are[30]:

a) derivation of clock information from a primary or secondary standard; for example, the transmitter and receiver can be slaved to a master clock through a separate channel.

b) transmitting a synchronising clock signal over the same channel as the signal.

c) derivation of the clock signal from the received waveform itself.

The first method is often employed in large data communication networks. Due to the high cost of this method, point-to-point data transmission normally does not use this method. A more economical method is to transmit the clock signal along with data, which means that a small part of the channel's information capacity needs to be used for the clock signal. The third method, known as self-synchronisation, is a very efficient method of synchronisation between receiver and transmitter. It uses a clock recovery network at the receiver to derive the clock signal (or pulse repetition frequency) from the received waveform or, in other words, from the the baseband information signal itself. It is this method that will be pursued and investigated in this project.

Extraction of the clock signal from the received signal waveform requires that the signal waveform contain sufficient timing information that the clock signal can be accurately reconstructed. The timing content will depend on the code format that is used to transmit the message signal. Code formats which provide enough transitions from which the receiver can recover both the clock signal and the data have been referred to as self clocking codes[11]. As clock recovery circuits at the receiver usually employ signal processing in the frequency domain (a narrow bandpass filter), a useful comparison of the various code formats with regard to timing content can be made by considering their spectral density curves. The timing content of a signal can be defined as the relative power strength of the discrete frequency line spectrum at nf_0 where n is 1,2,3 ... and f_0 is the pulse repetition frequency, with respect to the continuous

part of the spectrum of the signal. Hence, clock recovery at the receiver is basically a process which extracts the fundamental or the higher harmonics of the pulse repetition frequency from the signal.

At the transmitting end, it may be assumed that the signal elements are transmitted at a uniform rate. As the signal is transmitted along the fiber, the effects of fiber dispersion and receiver noise will destroy the original timing uniformity of the signal. These deviations from regular timing is known as timing jitter. Like other functions of time, the timing jitter function $j(t)$, can be associated with mean and r.m.s. values, and its Fourier transform function $J(\omega)$ describes the spectral distribution of the timing jitter. Hence, the spectral distribution of the signal at the receiver will consist of the spectral lines at nf_0 and the continuous spectrum contributed from the spectrum of the transmitted signal, together with that of the timing jitter.

Clock recovery at the receiver can be done by extracting a discrete component of the signal spectrum at the pulse-repetition frequency or its higher harmonics. This component may be extracted by a narrow-band, high Q, bandpass filter,a SAW device, or a phase-locked loop (PLL), to produce the clock signal to time the decision circuit of the receiver. However, this output clock signal will inevitably have phase variations or jitter since, although a high Q bandpass filter or PLL may have a very narrow bandwidth, it is still finite, and therefore cannot remove jitter frequencies which lie within its bandwidth. In addition, another source of clock jitter, known as pattern dependent jitter can result when timing recovery circuits are required to process digital signals that contains periods of minimal signal transitions. During these periods, the filter output decays and changes phase, particularly if it is not tuned exactly to the pulse repetition frequency or one of its harmonics. For PLL circuits, the output will drift to its free-running frequency during periods of no signal transitions, which also causes pattern dependent jitter, if the free-running frequency is mistuned from the input frequency.

In this chapter, a comparison is made among the spectra of analog Pulse Amplitude Modulation (PAM), Pulse Position Modulation (PPM), and Pulse Width Modulation(PWM), in terms of their timing content. No attempts are made here to derive the spectra for multilevel PAM, PPM and PWM as they can be quite difficult. However, qualitative deductions are made from the results obtained from the spectra of the analog pulse modulation, where the modulating signal is a sinusoid. This chapter will also introduce the various jitter parameters and derive the jitter tolerance for 4-level PAM and PWM systems. The advantages and

disadvantages of the use of a PLL compared to a tuned circuit in the clock recovery (timing extraction) process are also discussed.

4.2 Existence of Timing Signal

This section presents and compares the spectral content of sinusoidally modulated PAM, PPM and PWM code formats. As will be seen, PWM has the strongest timing content in its spectrum. These results are extended to qualitatively illustrate the relative strength of timing contents of quantized or multilevel PAM, PPM and PWM.

4.2.1 Spectra of Analog PAM, PPM and PWM

1) Spectrum of PAM

Consider the periodic unit impulse train

$$c_\delta(t) = \sum_{m=-\infty}^{\infty} \delta(t - mT) \qquad (4.1a)$$

$$where\ c_\delta(t + T) = c_\delta(t) \qquad (4.1b)$$

$c_\delta(t)$ may be expressed in Fourier series form as

$$c_\delta(t) = \sum_{m=-\infty}^{\infty} \delta(t - mT)$$

$$= \frac{1}{T} \sum_{n=-\infty}^{\infty} e^{jn2\pi f_0 t} \qquad (4.2a)$$

$$where\ f_0 = 1/T \qquad (4.2b)$$

Similarly, for a series of equally spaced arbitrarily shaped pulses,

$$c(t) = \sum_{m=-\infty}^{\infty} p(t - mT) \qquad (4.3a)$$

$$where\ c(t + T) = c(t) \qquad (4.3b)$$

$$\text{and } P(f) = \int_{-\infty}^{\infty} p(t)\, e^{-j2\pi ft} dt \qquad (4.3c)$$

which is the Fourier integral of p(t). Therefore,

$$c(t) = \sum_{m=-\infty}^{\infty} p(t - mT)$$

$$= \frac{1}{T} \sum_{n=-\infty}^{\infty} P(nf_0) e^{jn2\pi f_0 t} \qquad (4.4)$$

Equation (4.4) may be considered as the response of a filter with transfer function P(f) to the function $c_\delta(t)$ of (4.2).

Consider next a general signal s(t), assumed to be bandlimited to the band $|f| < W$; that is,

$$S(f) = 0\,, \quad |f| > W \qquad (4.5a)$$

$$\text{where } T = 1/(2W) \qquad (4.5b)$$

$$\text{and } f_0 = 2W \qquad (4.5c)$$

Ideally, the sampled s(mT) is transmitted via the impulse train,

$$x_\delta(t) = \sum_{m=-\infty}^{\infty} s(mT)\delta(t - mT) \qquad (4.6)$$

In practice, with an arbitrary pulse shape p(t),

$$x(t) = \sum_{m=-\infty}^{\infty} s(mT)p(t - mT) \qquad (4.7)$$

can be taken as representing the signal s(t).

The pulse p(t) may be obtained by assuming a unit impulse $\delta(t)$ being transmitted through a filter with transfer function P(f), where P(f) is the Fourier transform of p(t). Hence,

$$x(t) = p(t) * x_{\delta}(t) = p(t) * s(t)c(t) \qquad (4.8)$$

To illustrate with an example, let us use a sinusoidal waveform as the modulating signal and let the sampling performed by rectangular pulses, as depicted in Fig.4.1.

If the modulating wave is given by $A\cos 2\pi f_s t$, then the spectra of the PAM(RZ format) as given by Black[31] is (see Appendix A),

$$x(t) = \left[\Gamma A \sum_{m=-\infty}^{\infty} \frac{\sin \Gamma\pi \dfrac{mf_0 + f_s}{f_0}}{\Gamma\pi \dfrac{mf_0 + f_s}{f_0}} \cos\{2\pi (mf_0 + f_s)t\} \right] + \left[D\Gamma \sum_{m=-\infty}^{\infty} \frac{\sin m\Gamma\pi}{m\Gamma\pi} e^{j2\pi m f_0 t} \right] \qquad (4.9a)$$

$$\text{where } \Gamma = t_o/T \qquad (4.9b)$$

and D is a multiplier for the d.c. component. For $t_o = T$ (4.9) becomes,

$$x(t) = \left[A \sum_{m=-\infty}^{\infty} \frac{\sin \pi \dfrac{mf_0 + f_s}{f_0}}{\pi \dfrac{mf_0 + f_s}{f_0}} \cos\{2\pi (mf_0 + f_s)t\} \right] + D \qquad (4.10)$$

FIG. 4.1: PAM WITH RZ FORMAT

That is, when $t_o = T$, as usually is the case for multilevel or quantised PAM, the spectral line at f_s is not present.

2) Spectrum of PPM (with uniform sampling)

Consider the unmodulated pulse trains as from (4.3)

$$c(t) = \sum_{m=-\infty}^{\infty} p(t - mT) \qquad (4.11)$$

The different pulses in the wave of (4.11) must be strictly non-overlapping. Using the signal sample s(mT) to modulate the position of the m^{th} pulse of (4.11), the following PPM expression can be obtained:

$$x(t) = \sum_{m=-\infty}^{\infty} p\{t - mT - s(mT)\} \qquad (4.12a)$$

$$where\ p(t) = 0\ \ for\ |t| > T/2 - |s(t)|_{max} \qquad (4.12b)$$

$$or\ |s(t)|_{max} < T/2 \qquad (4.12c)$$

The closer $|s(t)|_{max}$ is to one half the pulse period T/2, the narrower must be the signal pulses in order that they will not interfere, and hence the wider the bandwidth that will be needed by the PPM signal x(t).

To simplify the analysis, let us use the unit impulse as the basic pulse shape p(t).

$$Therefore,\ x_\delta(t) = \sum_{m=-\infty}^{\infty} \delta\{t - mT - s(mT)\} \qquad (4.13a)$$

$$where\ |s(t)|_{max} < T/2 \qquad (4.13b)$$

Again, let us use a sinusoidal waveform as the modulating signal; that is,

$$s(t) = A\cos 2\pi f_s t \qquad (4.14a)$$

$$where\ A < T/2 \qquad (4.14b)$$

In determining the spectrum of $x_\delta(t)$, the double Fourier series of Bennett could be used and the final result as presented by Rowe[32] is

$$x_\delta(t) = \sum_{m=-\infty}^{\infty} \delta(t - mT - A\cos 2\pi f_s mT) \qquad (4.15)$$

$$= \frac{1}{T} \sum_{m=-\infty}^{\infty} \sum_{n=-\infty}^{\infty} (-j)^n J_n\{2\pi A(mf_0 + nf_s)\} e^{j2\pi(mf_0 + nf_s)t} \qquad (4.16a)$$

$$where\ f_0 = 1/T \qquad (4.16b)$$

and J_n is the usual Bessel function.

The sinusoidally modulated PPM using an impulse train contains discrete frequency components at all sum and difference frequencies of the modulating signal and the pulse repetition frequency, and their harmonics. Again, there is no obvious spectral line at the pulse repetition frequency or its harmonics.

Equation (4.16) can be generalised by using an arbitrary pulse shape for p(t). Therefore,

$$x(t) = \sum_{m=-\infty}^{\infty} p\{t - mT - \varepsilon(mT)\}$$

$$= \frac{1}{T} \sum_{m=-\infty}^{\infty} \sum_{n=-\infty}^{\infty} (-j)^n J_n\{2\pi A(mf_0 + nf_s)P(mf_0 + nf_s)\} e^{j2\pi(mf_0 + nf_s)t} \quad (4.17a)$$

$$\text{where } f_0 = 1/T \quad (4.17b)$$

3) Spectrum of PWM(with uniform sampling)

There are three ways to modulate a PWM signal. They are: 1)modulating the trailing edge, 2)modulating the leading edge and 3)modulating both the trailing edge and leading edge. In practice, the first method is easiest to achieve and hence we will only obtain the spectra for this type of modulation. The spectra of a sinusoidally modulated PWM signal using ideal rectangular pulses with a modulated trailing edge can be determined as follows:

$$\ell(t) = \sum_{m=-\infty}^{\infty} q(\varepsilon_m ; t - mT) \quad (4.18a)$$

$$\text{where } \ell(t) = 0 , \quad t < -T/2 \quad (4.18b)$$

$$\text{and } q(\varepsilon_m ; t) = 1 , \quad -T/2 < t < \varepsilon_m \quad (4.18c)$$

$$q(\varepsilon_m ; t) = 0 , \quad \varepsilon_m < t \quad (4.18d)$$

$$\varepsilon_m = \varepsilon(mT) \quad (4.18e)$$

$$|\varepsilon(t)|_{max} < T/2 \quad (4.18f)$$

$$\text{Let } s(t) = A\cos 2\pi f_s t \tag{4.19a}$$

$$\text{where } A < T/2 \tag{4.19b}$$

$$\text{Since } c_\delta(t) = \sum_{m=-\infty}^{\infty} \delta(t - mT) \tag{4.20a}$$

$$= \frac{1}{T} \sum_{m=-\infty}^{\infty} e^{jm2\pi f_0 t} \tag{4.20b}$$

$$\text{where } f_0 = 1/T \tag{4.20c}$$

$$\text{and } x_\delta(t) = \sum_{m=-\infty}^{\infty} \delta\{t - mT - s(mT)\} \tag{4.21a}$$

$$\text{for } |s(t)|_{max} < T/2 \tag{4.21b}$$

$$\text{Therefore } \frac{d}{dt}\ell(t) = c_\delta(t + T/2) - x_\delta(t) \tag{4.22}$$

Hence the expression for $\ell(t)$ is obtained by integrating (4.22) to give [32]

$$\ell(t) = \left[\frac{1}{T} \sum_{\substack{m=-\infty \\ m\neq 0}}^{\infty} (-1)^m \frac{e^{j2\pi m f_0 t}}{j2\pi m f_0}\right] - \left[\frac{1}{T} \sum_{\substack{m=-\infty \\ |m|+|n|\neq 0}}^{\infty} \sum_{n=-\infty}^{\infty} \frac{(-j)^n J_n\{2\pi A(mf_0 + nf_s)\}}{j2\pi(mf_0 + nf_s)} e^{j2\pi(mf_s + nf_s)t}\right] + 1/2 \tag{4.23a}$$

$$\text{where } f_0 = 1/T \tag{4.23b}$$

$$\text{and } A < T/2 = 1/(2f_0) \tag{4.23c}$$

From (4.23a), one can readily observe that the first term carries the spectral lines of the pulse repetition frequency and its harmonics. The third term of the same equation is the d.c. component of the PWM signal which is not necessarily 1/2 but depends on the modulating signal.

Comparing the spectra of the three pulse modulation techniques, one observes that PWM with a modulated trailing edge has the strongest line spectra at its pulse repetition frequency. For PAM to have distinctive line spectra in its pulse repetition frequency, it has to employ the RZ format, which would require a broader channel bandwidth. This RZ format is normally not used in quantised or multilevel PAM, where bandwidth conservation is a major factor. In the case of PPM, the larger the signal s(t), the less closely does the PPM signal resemble a periodic signal.

4.2.2 Advantages of Multilevel PWM for Clock Recovery

In the last section, the spectra of analog PAM, PPM and PWM are compared. A spectral comparison for quantized PAM, PPM and PWM modulated by random data, however, is beyond the scope of this thesis and no attempt is made to derive them. Instead, an analogy is drawn with the results from the sub section 4.2.1. In this earlier section, the spectra of the three pulse techniques modulated by sine wave, were presented. To simplify the analysis for the case of quantized or multi-level pulse modulation, the pulses can be assumed to be modulated by an analog signal s(t) whose amplitude only changes by discrete step(s) at the point of sampling, as depicted in Fig.4.2. The spectra for all three modulation techniques depends on the randomness of the modulating signal. The more random the modulating signal, the more continuous the nature of the spectra will be. In all three cases of PAM, PPM and PWM, their spectra are basically made up of the sum and difference of the modulating signal and the pulse repetition frequency and its higher harmonics. For a sinusoidal modulating signal, the spectrum will be made up of discrete spectral lines. As the modulating signal becomes more random in nature, these discrete spectral lines will become increasingly dense until, ultimately, they form a continuous spectrum. In the case of PWM(as well as for RZ PAM) there is another extra term

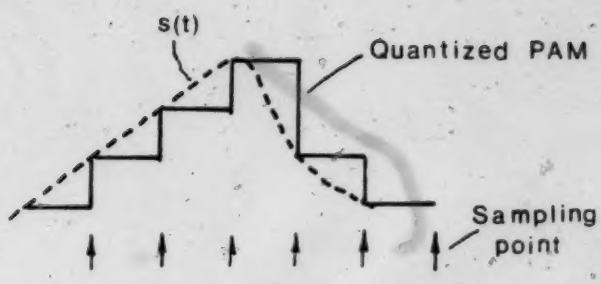


FIG. 4.2: QUANTISED PAM

in the spectrum(see (4.23a)) that carries the spectral line of the pulse repetition frequency, which is independent of the signal modulation. So, no matter how random the signal modulation is, the timing content remains unaffected.

From a practical point of view, for the extraction of the clock signal, PWM is the most convenient. This can be illustrated in Fig.4.3. It can be seen that PWM has the most consistent timing content, because of its fixed leading edge. PAM also has a fairly consistent transition for providing a timing signal, provided that the modulating signal changes sufficiently frequently and that the system characteristics do not distort the spacing between the rising and falling transition edges too greatly. In the case of PPM, the phase is modulated by the information signal and the more random the information, the more inconsistent the phase difference between two pulses will be, and hence the more difficult it becomes to extract the clock signal. Among all these, PWM offers the easiest approach for extracting the timing signal. All that is needed is a one-shot monostable, triggered on the rising edge of the PWM signal, as depicted in Fig.4.4. Much work has been done on the extraction of the clock signal from two-level PAM but not yet for the case of multilevel PAM[33,34]. The non-linear technique needed for extracting the clock information from multi-level PAM will be even more complicated than for

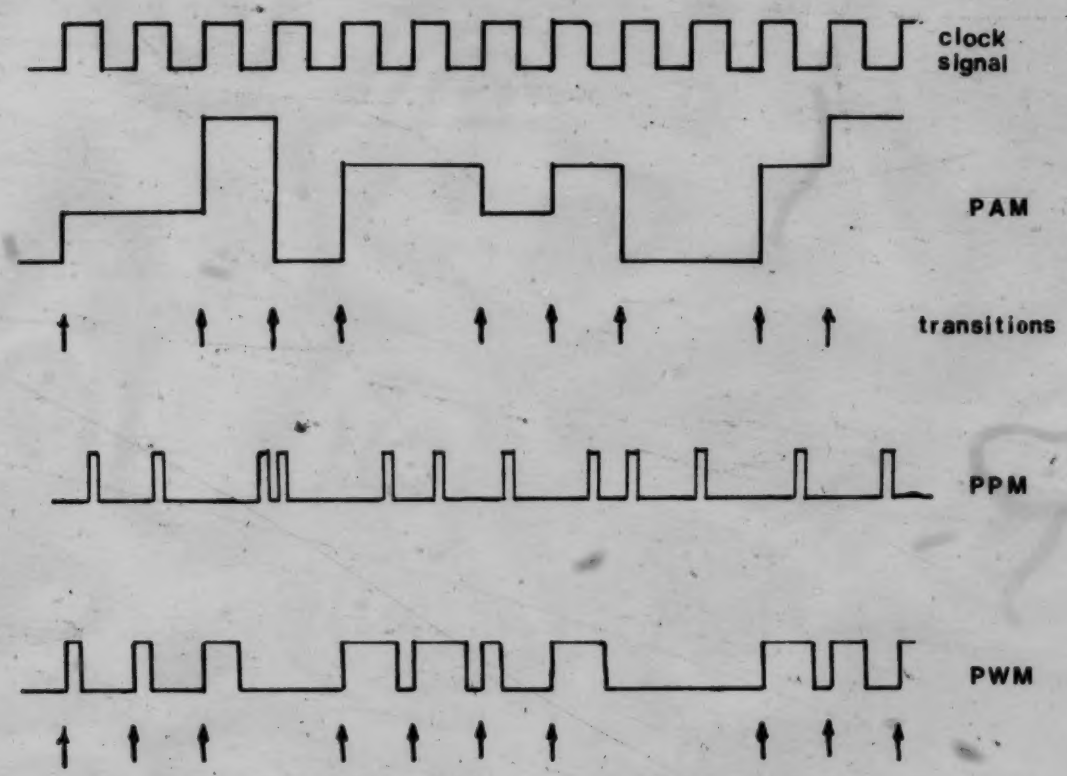


FIG. 4.3: CLOCK SIGNAL IN 4-LEVEL PULSE MODULATION

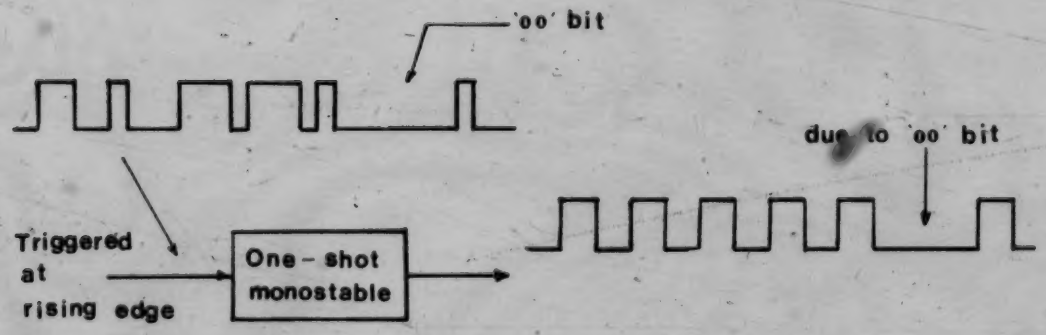


FIG.4.4: CONVERSION OF PWM TO CONSTANT WIDTH PULSES

two-level PAM, as the transitions of the signal do not take place at the same level. It is equally clear that the extraction of the clock signal from PPM would call for an even more complex technique, for example such as that presented by Gagliardi[35].

4.3 Jitter and its Parameters

The CCITT describes jitter as "short term variations of the significant instants of a digital signal from their ideal position in time"[36]. Jitter can in general be considered as a form of phase noise present on the digital signal. In this section, we will describe in greater detail the above general definition of jitter, covering some jitter parameters and giving a quantitative treatment of jitter tolerance for various code formats, including the 4-level PWM system.

4.3.1 Effects of Jitter

Timing jitter introduces transmission impairment in two ways:

a)During the process of regeneration, timing irregularity may displace the decision instant from the point of maximum eye opening of the signal, thus leading to a reduction in the noise margin and a degradation in the error rate performance. It should be noted, however, that the local timing extraction circuits employed in the regenerators may, at least to some extent, follow the timing variation in the incoming information signal, and this must be considered when assessing the effects on the error rate.

b) In the case of a digitally encoded analog signal, jitter leads to the decoded analog samples being spaced irregularly, thus introducing distortion into the baseband filtered signal.

4.3.2 Defining Peak-to-Peak Jitter

Peak-to-peak jitter may be defined as the maximum displacement of the n^{th} bit or symbol with respect to its position in a hypothetical unjittered reference stream[37]. The units may be in seconds, bits, or unit intervals. To illustrate this with an example, consider a sinusoidal periodic jitter with modulating rate f_i , bit rate f_s and a peak frequency deviation of the bit-rate, Δf (see Fig.4.5).

Let x be the number of bits occuring in the complete negative half of the jitter modulating waveform.

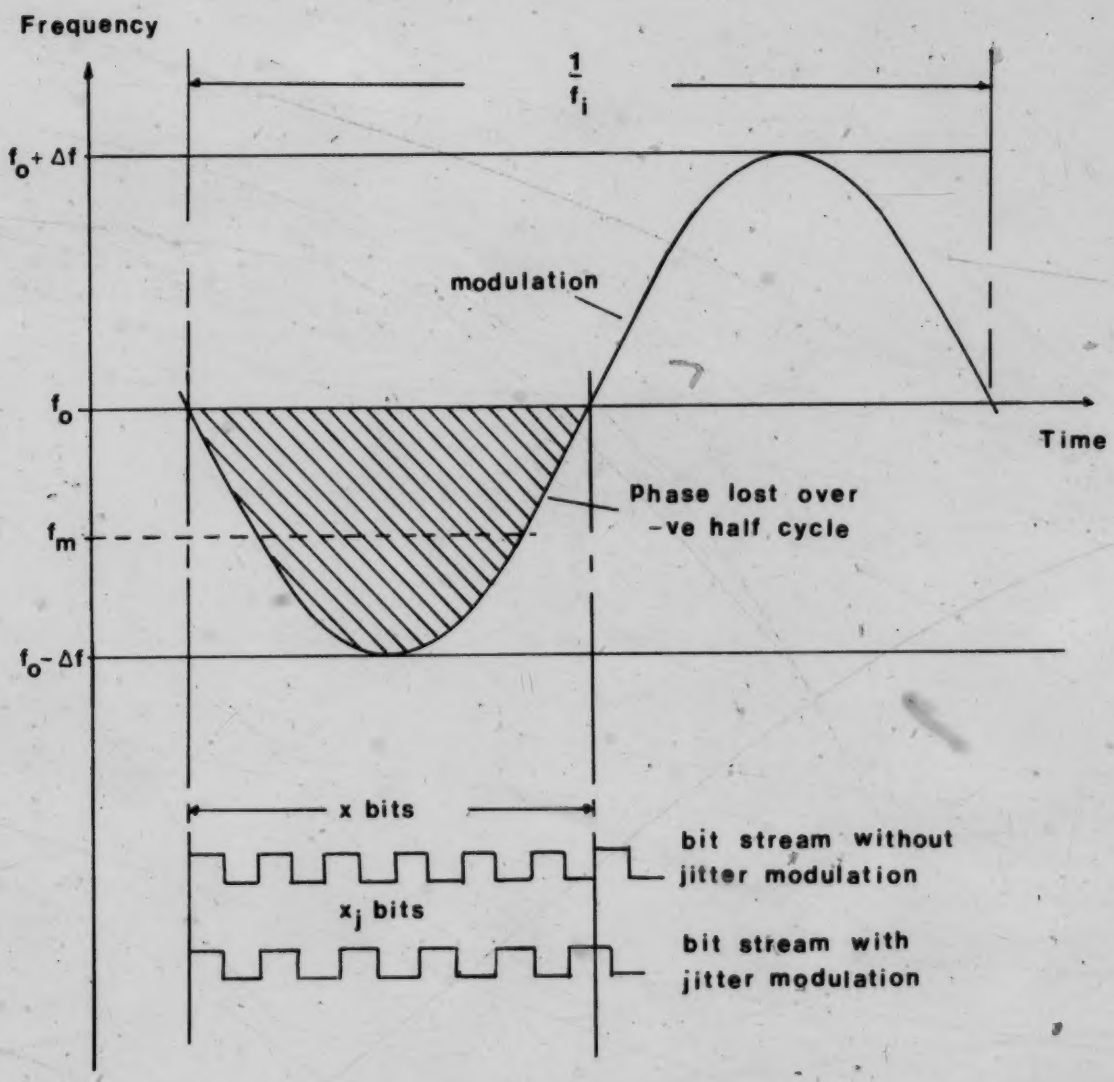


FIG. 4.5: SINUSOIDAL JITTER MODULATION

$$x = f_0 \frac{1}{2f_i} \quad bits \tag{4.24}$$

where $1/(2f_i)$ is the one-half period of the jitter modulating waveform and f_0 is the bit rate without jitter. The mean bit rate with jitter for the negative half cycle is

$$f_m = f_0 - \Delta f \frac{1}{\pi} \int_0^{\pi} sin\theta d\theta$$

$$= f_0 - \frac{2}{\pi}\Delta f \tag{4.25}$$

Therefore, during the negative half period, the number of bits occurring with jitter is

$$x_j = f_m \frac{1}{2f_i} = (f_0 - \frac{2}{\pi}\Delta f) \frac{1}{2f_i} \quad bits \tag{4.26}$$

Hence, the peak-to-peak jitter, in term of bits is

$$J_{pp} = x - x_j \tag{4.27}$$

$$Therefore, \quad J_{pp} = \frac{f_0}{2f_i} - (f_0 - \frac{2}{\pi}\Delta f) \frac{1}{2f_i}$$

$$= \frac{2}{\pi} \frac{\Delta f}{2f_i} = \frac{\Delta f}{\pi f_i} \quad bits \tag{4.28}$$

In terms of seconds with reference to the bit rate f_0,

$$J_{pp} = \frac{\Delta f}{\pi f_i} \frac{1}{f_0} \quad secs. \tag{4.29}$$

Peak-to-peak jitter is proportional to the peak deviation Δf and inversely proportional to the jitter frequency. It is also a function of the jitter modulating function.

4.3.3 Jitter Parameters

1) *Jitter Tolerance*

This is the amount of jitter a system can tolerate at its input. For illustration purposes, a simple binary RZ code format will be used. The parameter which is of major importance is the maximum run of zeros allowed in the code. For the case where a phase locked loop(PLL) is used as the clock extraction device, it will resonate at its natural frequency in the absence of data marks, but it is updated in phase during the presence of data marks. If a tuned circuit is used instead, it has to have a sufficiently high Q factor to oscillate for the period of the zero-block.

Consider again a sinusoidal jitter function; the worst case occurs when the block of zeros occurs at the point of maximum deviation of the jitter modulation, as depicted in Fig.4.6. The time domain limitation to the process of clock recovery is determined by the maximum phase error which occurs at the point of maximum phase error which can be allowed to accumulate during the run of zeros. This phase error is measured between the sampling clock and the first data mark to occur at the end of the zero block. For simplicity of analysis, the PLL or tuned circuit is assumed to run at its free running frequency(ideally at the bit rate) during the data zeros. In the case of a RZ code format, the maximum allowable phase deviation over a block of zeros is one-half of the data pulse width, and for centrally sample data, it is therefore, 1/4 bit(see Fig.4.6). Referring to Fig.4.7, the average frequency of the data during a n-bit zero block is

$$f_{av} = f_0 - \left[\frac{2\Delta f \int_{\frac{\pi}{2}(1-\frac{n+1}{x})}^{\frac{\pi}{2}} \sin\theta d\theta}{\pi \frac{n+1}{x}} \right] \qquad (4.30)$$

where x is the number of bits occuring in the complete -ve half of the modulating waveform. The time take for (n+1) bits in terms of the bit rate f_0 is

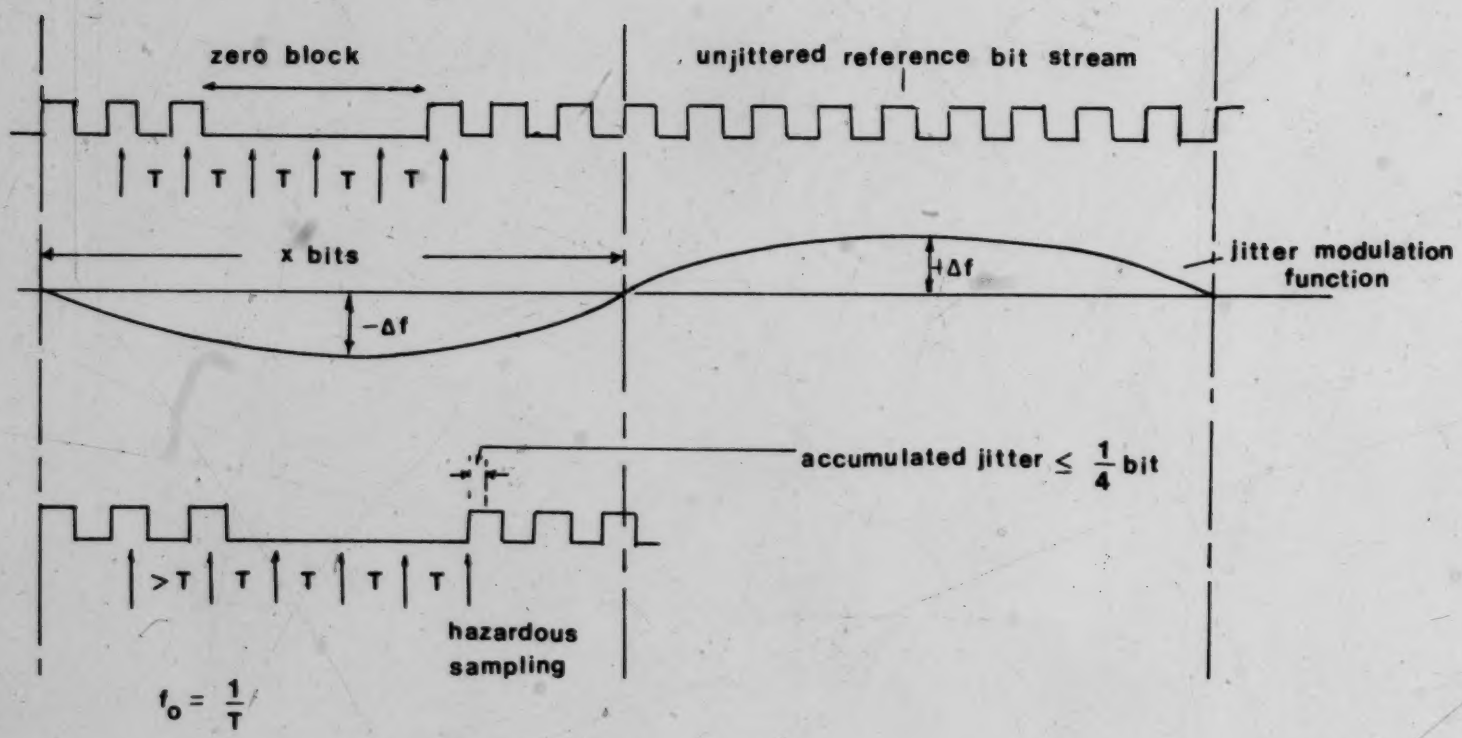


FIG. 4.6 : ZERO BLOCK IN NEGATIVE HALF MODULATION PERIOD

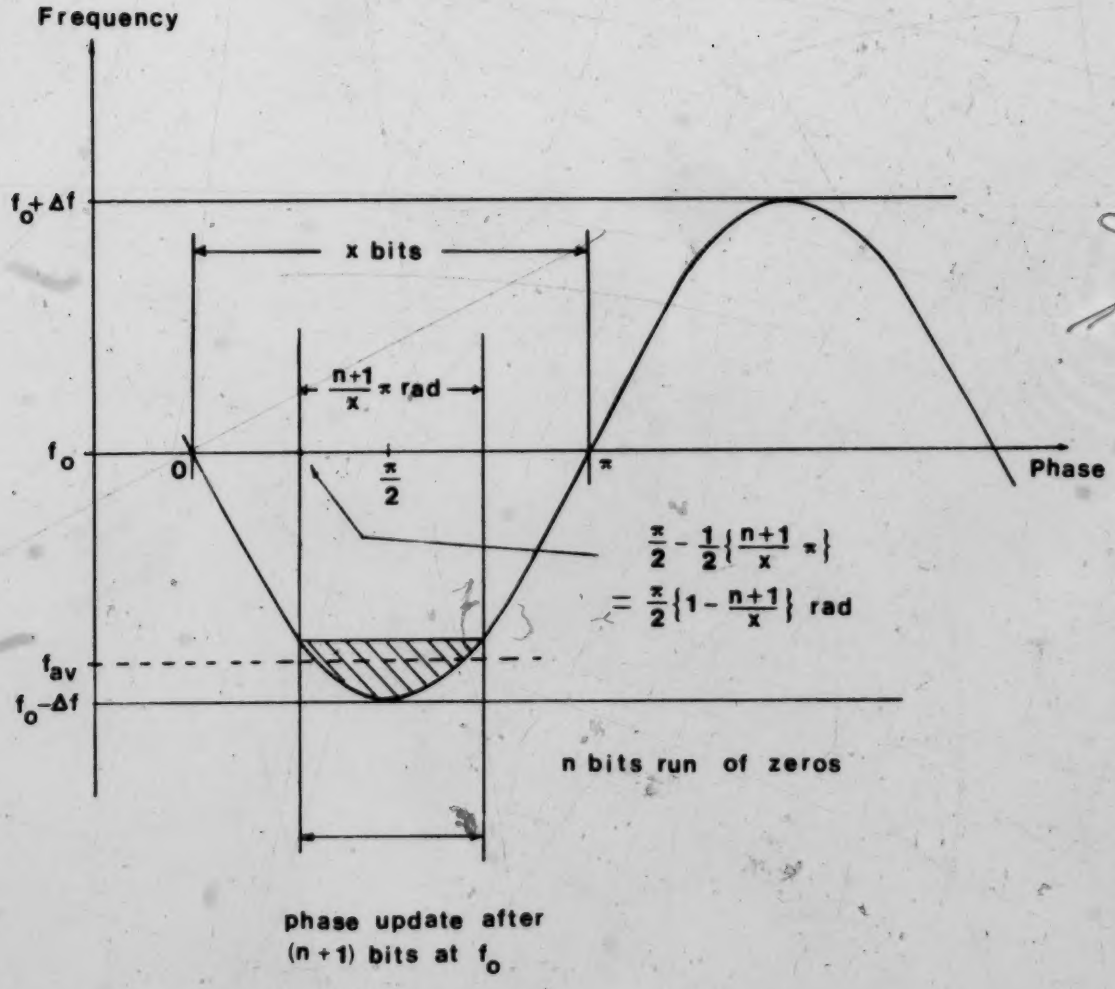


FIG. 4.7: CLOCK RECOVERY LIMITATION

$$t_{n+1} = \frac{n+1}{f_0} \quad secs. \tag{4.31}$$

Therefore the number of bits with jitter modulation during t_{n+1} sec is

$$n_i = f_{av} \frac{n+1}{f_0}$$

$$n_i = f_{av} t_{n+1} = f_{av} \frac{n+1}{f_0} \tag{4.32}$$

For the RZ data format, 1/4 bit is the maximum allowable phase error.

$$Hence, \quad (n+1) - n_i < 1/4 \tag{4.33}$$

$$or \quad (n+1) - f_{av} \frac{n+1}{f_0} = 1/4$$

which gives

$$1/4 = (f_0 - f_{av}) \frac{n+1}{f_0} \quad bit \tag{4.34}$$

Substituting (4.30) into (4.34),

$$1/4 = \frac{2\Delta f x}{\pi f_0} \cos\frac{\pi}{2}(1 - \frac{n+1}{x}) \quad bit \tag{4.35}$$

$$or \quad \Delta f = \frac{1}{4} \frac{\pi f_0}{2x\cos\frac{\pi}{2}(1 - \frac{n+1}{x})} \tag{4.36}$$

From (4.24) and (4.29),

$$J_{pp} = \frac{2}{\pi} \Delta f \frac{x}{f_0} \quad bits \tag{4.37}$$

So, substituting (4.36) into (4.37),

$$J_{pp} = \frac{1}{4} \frac{1}{\cos\frac{\pi}{2}(1 - \frac{n+1}{x})} \quad bits \tag{4.38a}$$

$$where\ x = f_0/(2f_i) \tag{4.38b}$$

From (4.24),(4.36),(4.38),

$$\Delta f = \pi f_i J_{pp} \tag{4.39}$$

Equations (4.38) and (4.39) are valid provided

$$\frac{n+1}{x} < 1 \tag{4.40}$$

If $\frac{n+1}{x} \geq 1$, zeros can always fill a complete half period of f_i . Henceforth, only 1/4 bit may be accumulated during this time.

$$Therefore,\ J_{pp} = 1/4 \quad for \quad \frac{n+1}{x} \geq 1 \tag{4.41}$$

$$\Delta f = \frac{\pi}{4} f_i \quad for \quad \frac{n+1}{x} \geq 1 \tag{4.42}$$

It is important to note that n is the maximum number of zeros in a block. The signal can have a number of zeros smaller than n, but not greater.

So far, the derivation for jitter tolerance has been for RZ data format. For NRZ data format, such as in multilevel PAM (where $t_o = T$), the jitter tolerance is doubled, both for $\frac{n+1}{x} < 1$ and for $\frac{n+1}{x} \geq 1$ (see Fig 4.8)

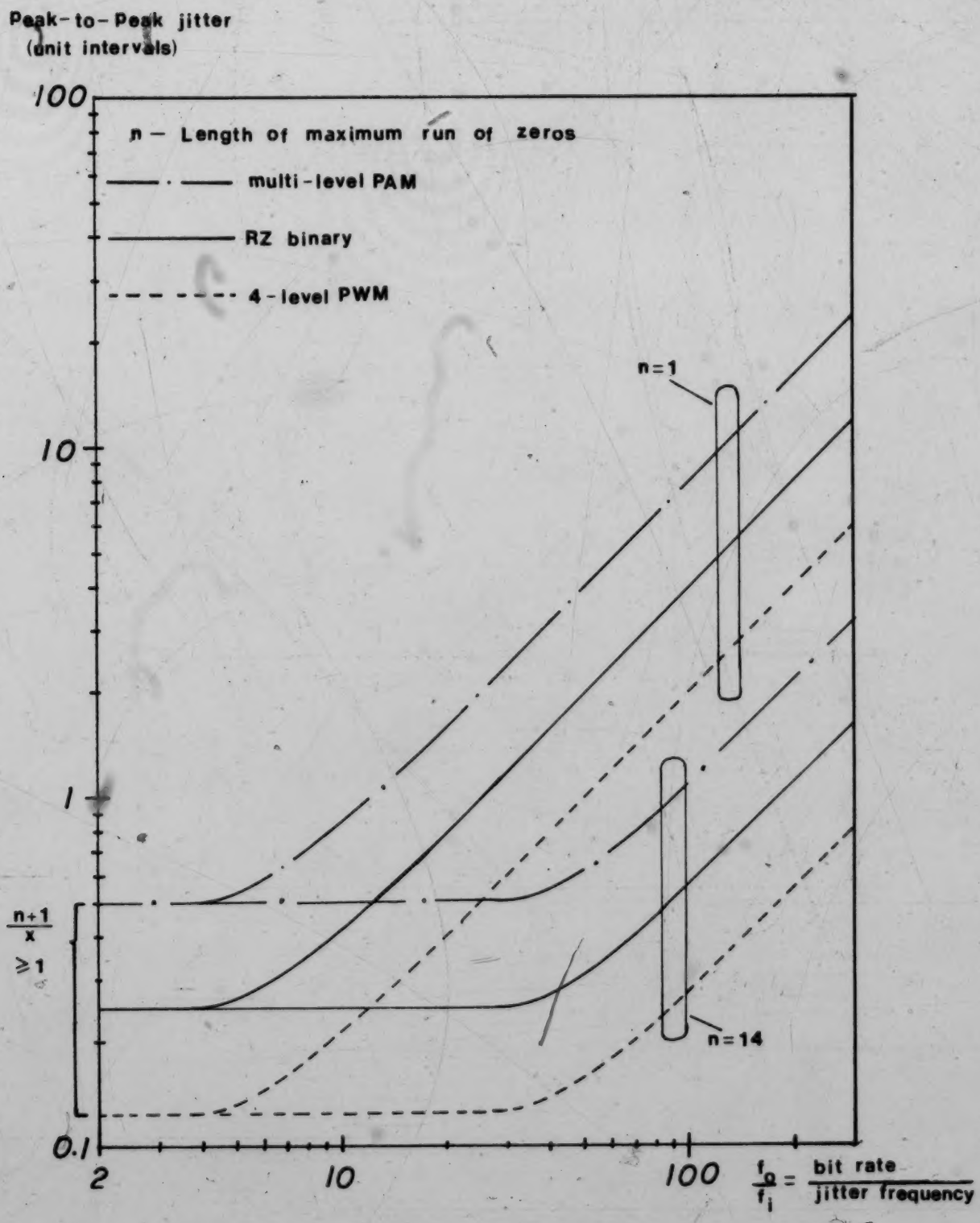


FIG. 4.8 : FUNDAMENTAL TIME DOMAIN JITTER TOLERANCE LIMITS

As for the 4-level PWM format used in this project, its smallest pulse width is 1/2 the value of that of the RZ format, hence its jitter tolerance is also reduced by 1/2.

$$J_{pp} = \frac{1}{8} \frac{1}{\cos\frac{\pi}{2}(1 - \frac{n+1}{x})} \quad for \ \frac{n+1}{x} < 1 \qquad (4.43)$$

$$and \ J_{pp} = \frac{1}{8} \quad for \ \frac{n+1}{x} \geq 1 \qquad (4.44)$$

It is important to note that the above derivations express the fundamental limits of jitter tolerance for different code formats and the calculation of this jitter tolerance was based on the assumption of ideal rectangular waveforms. In practice, the waveforms are distorted by noise and channel imperfections which will degrade the jitter tolerance. Furthermore, it is not easy to compare jitter tolerance for different code formats, as each code format requires different channel characteristics such as bandwidth and pulse shaping.

In summary, jitter tolerance depends on

1) Data code format
2) Maximum number of zeros in a block
3) Jitter function
4) Channel characteristics and
5) Acquisition behaviour of the the timing extraction device (which, due to its complex nature, is not considered here).

2) *Jitter Transfer*

a) Jitter Transfer Function

The jitter transfer function of a digital line describes the relationship between the applied input jitter and the resulting output jitter as a function of frequency. For a digital regenerator, the jitter transfer function is chiefly determined by the frequency characteristics of the timing recovery(extraction) circuit.

b) Jitter Peaking

Jitter peaking is the maximum jitter enchancement occurring in the jitter transfer function. Jitter peaking does not occur with timing extraction circuits using single tuned

circuits. However, many widely used second-order phase locked loops, if designed with underdamped performance, will exhibit some degree of peaking. Jitter peaking is undesirable in any long chain of similar digital repeaters, since it can result in exponential growth in the timing jitter[38].

3)*Jitter Generation*

Jitter generation is the amount of self-generated jitter produced by digital systems. Two well-known jitter generation mechanisms are systematic jitter and random jitter[39].

a) Systematic(pattern dependent) jitter

Systematic jitter is jitter chiefly produced in a timing extraction process correlated with the incoming data pattern. Causes of this jitter include intersymbol interference, mistuning of the timing extraction device free running frequency and amplitude-to-phase conversion[39].

b) Random Jitter

Sources of random jitter include channel noise, receiver noise and random mistuning of the timing extraction circuit. Random jitter accumulates less rapidly than systematic jitter in a chain of similar repeaters, since the sources in each repeater are uncorrelated.

4.4 Timing Extraction

Synchronizing the receiver clock with the incoming data is commonly achieved by processing the digital signal in such a way as to extract a suitable timing wave. A general block diagram of a timing extraction system is shown in Fig.4.9.

A linear filter may be used to shape the incoming signal as well as to limit system noise. The non-linear network is used to more efficiently extract the timing content from the signal. For example, the binary NZR code format signal has a null in the power spectrum at the pulse repetition frequency [40], and hence it does not directly contain a timing component. However, observation of the signal in the time domain shows that data transitions occur at definite time intervals which assures us of the presence of timing information (see Fig.4.10).

In Fig.4.10, the non-linear circuit employed is a differentiator with a full-wave rectifier. Pulse trains derived in this manner satisfy the criterion for the existence of timing

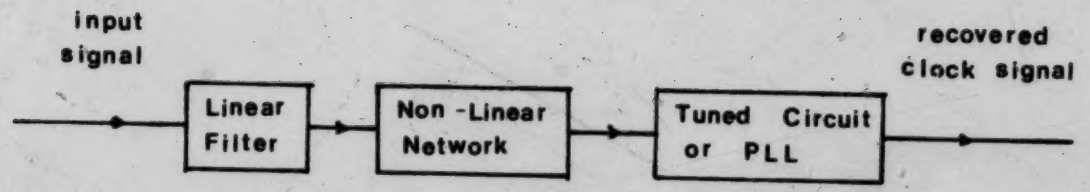


FIG. 4.9: A GENERAL TIMING EXTRACTION CIRCUIT

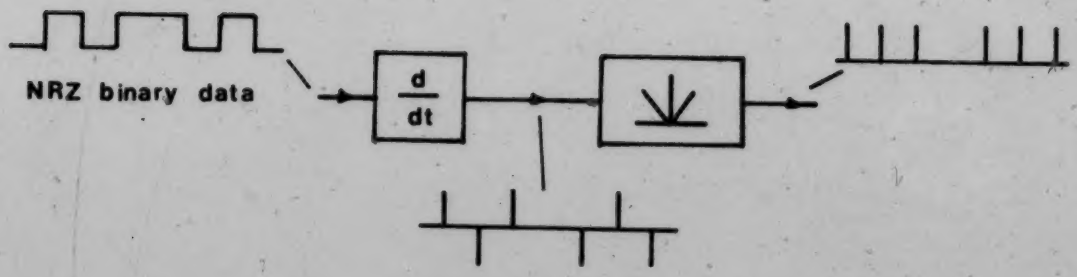


FIG. 4.10: DETECTION OF SIGNAL TRANSITION IN NRZ BINARY DATA

information. However, these pulse trains cannot be used directly as timing signals, since they still do not contain pulses in every time slot. To overcome this problem, a high-Q tuned circuit or PLL, tuned to the pulse repetitive frequency can be used to provide a regular repetitive train of clock pulses. As already mentioned, the two most commonly used timing extraction devices are the tuned circuit and the PLL. The following section treats each method in greater detail and a comparison is made to show that the PLL is the superior timing extraction device.

4.4.1 Tuned Circuit

Assume a series RLC combination is used that resonates at the angular frequency ω_r. Then the tank circuit transfer function will be [41],

$$Y_t(\omega) = \frac{1}{R + j(\omega L - \frac{1}{\omega C})} \qquad (4.45)$$

Consequently, the relative transmission of the signal element timing signal across the tuned circuit is given by

$$\frac{Y_t(\omega_r)}{Y_t(\omega_0)} = \frac{1}{1 + jQ(\lambda_r - \frac{1}{\lambda_r})} \qquad (4.46a)$$

$$where \quad Q = \frac{\omega_r L}{R} \qquad (4.46b)$$

$$and \ \omega_r = 1/(LC)^{1/2} \ \ rad/sec \qquad (4.46c)$$

$$and \ \lambda_r = \frac{f_0}{f_r} = \frac{\omega_0}{\omega_r} \qquad (4.46d)$$

and ω_0 is the pulse repetition angular frequency. The timing signal then experiences a phase shift ϕ defined by

$$\tan\phi = Q(\lambda_r - \frac{1}{\lambda_r}) \qquad (4.47)$$

$$If \quad |f_0 - f_r| = \Delta f_0 << f_0 \tag{4.48}$$

$$Then \quad \tan\phi = \frac{2Q\Delta f_0}{f_0} \tag{4.49}$$

where Δf_0 is known as the circuit mistune. In principle, the phase error is zero when $\Delta f_0 = 0$. In practice there is always some degree of mistuning, hence some static phase error is introduced.

A second and perhaps more serious problem associated with this mistuning is the jitter introduced by the tendency of the tuned circuit to drift towards its free running frequency in the absence of any transition of the signal waveform. This free running angular frequency is given by:

$$\omega_n = \left(\frac{1}{LC} - \frac{R^2}{4L^2}\right)^{1/2} \tag{4.50}$$

whose value is smaller than that of the resonant angular frequency of the circuit, which is given by $1/\sqrt{LC}$. In other words, even if the tuned circuit is correctly tuned, so that its resonant frequency equals to that of the pulse repetition frequency of the signal, there will still be drifting of frequency (as given by (4.50)) during the absence of any transition of the signal. However, as Q approaches infinity, $\omega_r = \omega_n$, so this drift tends to zero as the Q becomes very large.

In general, a tuned circuit exhibits some degree of mistuning and it has finite Q and hence it accepts contribution for tuning reference from three different sources:

1)The spectral line of f_0.

2)The continuous spectrum immediately about f_0.

3)Random components due to noise.

Let us consider the modulation of the carrier by the components in the continuous spectrum situated at frequencies within $f_0 \pm f_q$. The relative amplitudes of the two sideband components after transmission through the tuned circuit are:

$$\frac{\varepsilon_1}{\varepsilon} = \frac{1}{1 + jQ(\lambda_r + \lambda_q - \frac{1}{\lambda_r + \lambda_q})} \qquad (4.51a)$$

$$\text{and} \quad \frac{\varepsilon_2}{\varepsilon} = \frac{1}{1 + jQ(\lambda_r - \lambda_q - \frac{1}{\lambda_r - \lambda_q})} \qquad (4.51b)$$

$$\text{where } \lambda_q = \frac{f_q}{f_r} \qquad (4.51c)$$

It can be seen that the two sidebands now are no longer equal and, using standard techniques, the sidebands can be split up into a pair of symmetric and anti-symmetric components. The former introduces amplitude modulation while the latter introduces phase modulation of the carrier. In an ideal situation, a perfect threshold detector following the resonant tuned circuit would remove all amplitude modulation from the derived timing wave. But, in practice, the operating point of the threshold detector is often offset from zero, as shown in Fig.4.11a and Fig.4.11b. Then, any amplitude variation in the timing signal will result in a phase variation at the output of the limiter, giving rise to the amplitude-to-phase conversion problem.

4.4.2 Second-order PLL

Another commonly used timing extraction device is the phase locked loop. No attempt is made to elaborate on the principles of the PLL in this section. A more detailed treatment of the PLL is given in the next chapter.

The transfer function of a second-order PLL with a lag-lead filter is given by (see section 5.2.2)

$$H(s) = \frac{s\omega_n(2\zeta - \omega_n/K) + \omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \qquad (4.52)$$

where ω_n is the natural angular frequency, ζ is the damping factor and K is the loop gain.

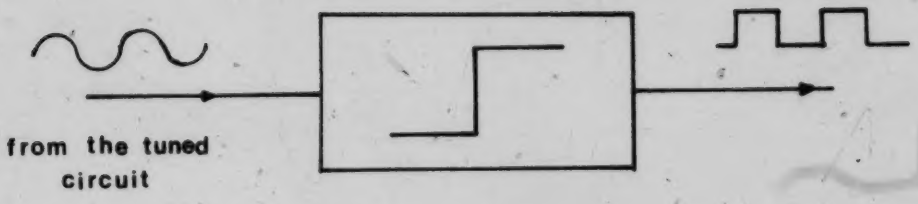


FIG. 4.11a: THE THRESHOLD DETECTOR CONVERTING A SINE WAVE INTO A SQUARE WAVE

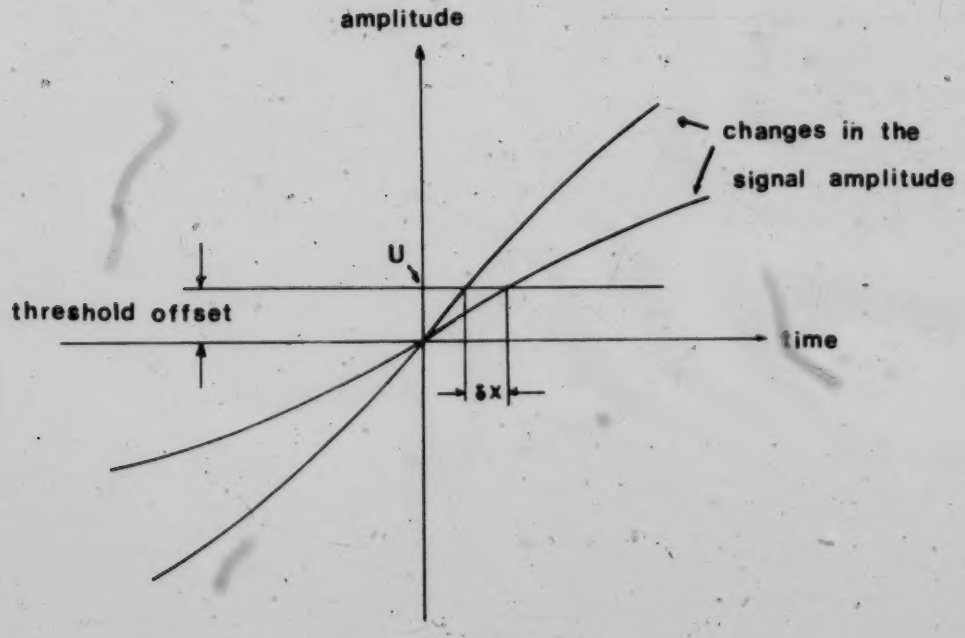


FIG. 4.11b: PRODUCTION OF TIMING JITTER BY THRESHOLD OFFSET. THRESHOLD, NORMALLY AT ZERO AMPLITUDE, IS OFFSET TO U.

The noise bandwidth for a high loop gain second-order PLL is given by (see section 5.4)

$$B_n = \frac{\omega_n}{8\zeta}(1 + 4\zeta^2) \qquad (4.53)$$

and the seize frequency, which is the maximum deviation of the signal frequency from the PLL free running frequency that can be captured without cycle slipping, is given by (see section 5.6)

$$\omega_s = \frac{\pi}{2}\omega_n^2 T_2 \qquad (4.54a)$$

$$\text{where } T_2 = R_2 C \qquad (4.54b)$$

where R_2 and C are components of the PLL filter. The static phase error for a given mistune (as in the tuned circuit) is given by

$$\theta_e = \frac{\Delta\omega}{K} \qquad (4.55)$$

where $\Delta\omega$ is the mistune in frequency due to temperature, aging, moisture and/or circuit offset.

Comparing (4.53) and (4.54), one can observe that, to narrow the noise bandwidth, ω_n has to be reduced; however, this also reduces the seize frequency of the PLL. The only somewhat independent parameter is seen to be the loop gain.

4.4.3 Comparison of Tuned Circuit and PLL for Clock Recovery

Comparing the properties of the two clock extraction devices, one can make the folowing points:

1) Reduction of static phase error is not easy to achieve with a simple resonant type circuit. From (4.49), one can observe that, for a given mistune, the static phase error increases with the Q factor. As most clock recovery circuits would require a high Q circuit to handle long runs of zeros as well to suppress timing jitter, a compromise is necessary. There is no such dependence in the case of a high gain second-order PLL. Equations (4.53) and (4.55) show that the noise bandwidth is independent of the gain of the loop. In other words, a small noise

bandwidth can be achieved together with a small static phase error.

2) In resonant type circuits, in contrast to the signal from the PLL, the derived clock signal is amplitude modulated. This modulation has to be removed by a threshold detector which, if not perfect, may introduce new phase error.

3) In the absence of signal transitions, the tuned circuit due to its internal energy storage will continue to oscillate and drift towards its natural frequency with an exponentially decaying amplitude until the next transition of the signal re-initiates the forced response of the tuned circuit. Again, if the threshold detector has some degree of zero offset, this decaying amplitude will cause "amplitude-to-phase" error. As jitter is pattern dependent, it will accumulate along a chain of similar repeaters. This problem can be overcome by the PLL with its constant amplitude output of the VCO, particularly those whose output is a square waveform.

4) The most obvious disadvantage of a second-order PLL is the possible peaking of its transfer function which can cause serious jitter accumulation along a chain of similar regenerators. This problem can be reduced by using a highly damped second-order PLL [42].

Since the cost of monolithic PLL circuits is decreasing, the use of PLL's for timing extraction is becoming more common. Its superior performance, as compared to the tuned circuit, however, requires more complicated procedures in the design and parameter optimization of the circuitry. A general monolithic PLL(XR215) was used in this project as a timing extraction device. In the next chapter, a more detailed analysis of the PLL is given.

Chapter 5

THE PHASE-LOCKED LOOP

One of the best known properties of the phase locked loop(PLL) is that of the restitution of the phase, and hence the frequency, of a signal immersed in noise, which can subsequently be detected coherently. With the cost of PLL's, particularly that of monolithic PLL's decreasing, their use in timing extraction circuits in receivers of a digital communication systems, has become common.

This chapter will outline the basic principles of the PLL and proceed to justify why the high gain second-order PLL with a lag-lead filter is preferred in clock recovery. The various PLL parameters such as noise bandwidth, loop gain, damping factor and how they affect its transient behaviour will be briefly discussed. No attempt is made to derive in detail the equation for the various PLL parameters, as this can be obtained from many textbooks [43,44].

5.1 Concepts

The elements of a phase locked loop system are a phase detector, a loop filter and a voltage-controlled oscillator(VCO), as depicted in Fig. 5.1. The frequency of the VCO is proportional to an externally applied voltage. Under the condition that the loop is locked onto an incoming periodic signal, the VCO frequency is exactly equal to that of the signal. The phase detector produces a d.c. or low-frequency signal proportional to the difference in phase between the incoming signal and the VCO input signal. This phase-dependent signal is then filtered, to be applied to the control input of the VCO in such a way as to drive the VCO frequency back to the same value as the incoming signal. Hence, the loop can maintain lock when the input signal changes its frequency, and the VCO input control voltage will adjust accordingly. The range of input frequencies over which the loop can maintain lock is defined as the 'locking range'. In the unlocked condition, the VCO operates at its free running frequency, which corresponds to zero applied d.c. voltage at its control input.

When a periodic signal is applied that has a frequency close to the free-running frequency, the loop may or may not lock onto it, depending on a number of factors. The capture process is inherently non-linear in nature. The capture range of the loop is that range of input frequencies around the free-running frequency of the VCO onto which the loop will

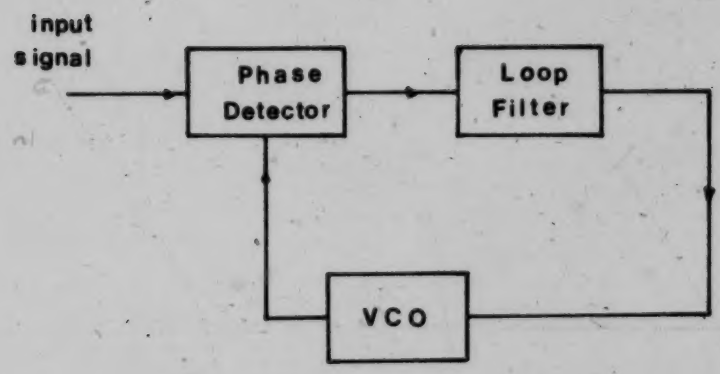


FIG. 5.1: A PHASE LOCKED LOOP

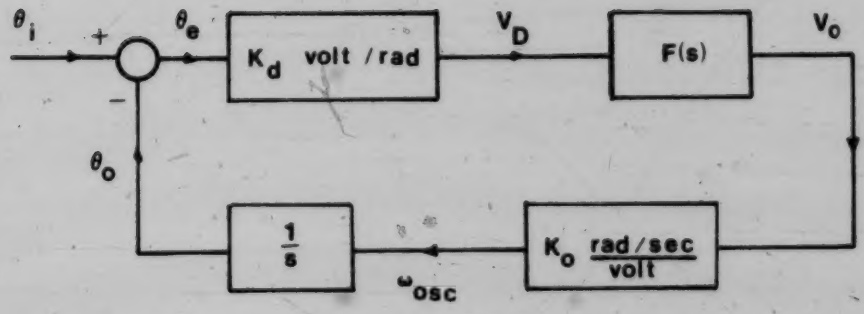


FIG. 5.2: BLOCK DIAGRAM OF A PLL

become locked, starting from an unlocked condition. The pull in time is the time required for the loop to "capture" the signal. Both these parameters depend on the bandwidth of the loop filter, as well as on the gain of loop itself[45]. The function of the filter is to smooth out difference components resulting from interfering signals far away from the free-running frequency. It also provides memory for the loop during moments when loop lock is lost due to a large interfering transient. Reducing the filter bandwidth improves the rejection of out-of-band signals, but at the same time this narrows the capture range and increasing the pull-in time.

5.2 The PLL in the Locked Condition

Consider the diagram shown in Fig. 5.2, for which the input signal has a phase of $\theta_i(t)$ and the VCO output has a phase $\theta_0(t)$. We assume that the loop is locked, that the phase detector is linear and that the phase detector output voltage is proportional to the difference in phase between its inputs; that is

$$V_D = K_d(\theta_i - \theta_0) \qquad (5.1)$$

where K_d is called the phase-detector gain factor(volts/rad).

The phase error voltage V_D is filtered by the loop filter F(s). The frequency of the VCO is determined by the control voltage V_c. If a constant input voltage is applied to the VCO control input, the output frequency of the VCO remains constant. The deviation of the VCO from its free-running frequency is $\Delta\omega = K_d V_D$, where K_c is the VCO gain factor(rad/sec-volt). The VCO operation may be described as

$$\omega_{osc(t)} = \frac{d\theta_0(t)}{dt} \qquad (5.2a)$$

$$\theta_0(t) = \theta_0|_{t=0} + \int_0^t \omega_{osc}(t)dt \qquad (5.2b)$$

This inherent integration is represented by the 1/s block in Fig. 5.2. The relation between the VCO output frequency ω_{osc} and V_0 is

$$\omega_{osc} = \omega_R + K_0 V_0 \tag{5.3}$$

where ω_R is the free-running frequency that results when $V_0=0$.

The system can be seen from Fig.5.2 to be a classical linear feedback control system. The basic loop equations are given by[46].

$$\frac{\theta_0(s)}{\theta_i(s)} = H(s) = \frac{K_0 K_d F(s)}{s + K_0 K_d F(s)} \tag{5.4}$$

where H(s) is the closed-loop transfer function.

$$\frac{\theta_i(s) - \theta_0(s)}{\theta_i(s)} = \frac{\theta_e(s)}{\theta_i(s)}$$

$$= 1 - H(s) = \frac{s}{s + K_0 K_d F(s)} \tag{5.5}$$

$$V_0(s) = \frac{s K_d F(s) \theta_i(s)}{s + K_0 K_d F(s)} = \frac{s\theta_i(s)}{K_0} H(s) \tag{5.6}$$

5.2.1 First Order Loop

We first consider the case in which the loop filter is removed entirely, that is $F(s)=1$. This is called a first-order loop, for which

$$\frac{\theta_0(s)}{\theta_i(s)} = H(s) = \frac{K_0 K_d}{s + K_0 K_d} = \frac{K}{s + K} \tag{5.7a}$$

$$\text{where } K = K_0 K_d \tag{5.7b}$$

Thus the loop inherently produces a first-order, low pass transfer characteristic. The constant K, which has the dimension of rad/sec, is known as the loop gain, which is also the effective bandwidth of the PLL. The root locus of this single pole as a function of loop gain K is shown in Fig5.3(a) and the corresponding frequency response is shown in Fig5.3(b).

Operating the loop with no filter has several practical drawbacks. Since the phase detector is really a multiplier, it produces a sum frequency component as well as a difference frequency component. The component at twice the frequency will be fed directly to the output if there is no loop filter. Also, all the out-of-band interfering signals present at the input will appear, shifted in frequency, at the output. As good tracking of the system depends on the gain K, the bandwidth has to be large. Hence, narrow bandwidth and good tracking are incompatible in the first-order loop, and for this reason it is not often used.

5.2.2 Second-order Loop

The most common configuration for monolithic PLLs is the second-order loop. Consider the case of a simple low pass filter, as shown in Fig.5.4. The transfer function for such a filter is

$$F(s) = \frac{1}{1 + sT_1} \qquad (5.8a)$$

$$\text{where } T_1 = RC \qquad (5.8b)$$

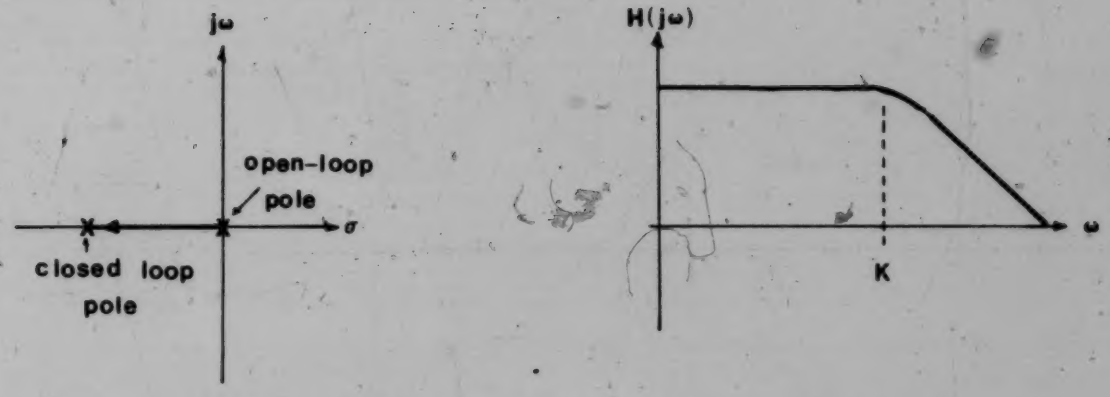
Substituting (5.8a) into (5.4), we obtain

$$H(s) = \frac{\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \qquad (5.9a)$$

$$\text{where } \omega_n = \sqrt{(K/T_1)} \qquad (5.9b)$$

$$\text{and } \zeta = 0.5\sqrt{1/(KT_1)} \qquad (5.9c)$$

A second-order loop PLL is basically characterised by 3 main parameters, namely: the natural angular frequency ω_n ,the damping factor ζ and the loop gain K. However, as



a) Root Locus

b) Closed Loop Response

FIG. 5.3: RESPONSES OF A FIRST-ORDER PLL

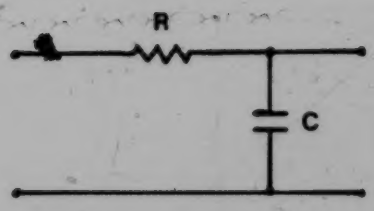


FIG 5 4: SIMPLE LOW-PASS FILTER

can be seen from (5.9), there are only two available circuit parameters namely: T_1 and K. Hence, as a result, the above 3 parameters cannot be chosen independently. For example, if it is necessary to have a large d.c. gain and a small bandwidth, the loop will be badly underdamped and the transient response will be poor. This will cause an enhancement of the jitter in clock recovery. By adding a zero to the loop filter, the pole can be made small while maintaing good loop damping. This can be achieved by the filter depicted in Fig.5.5. The transfer function for this filter is

$$F(s) = \frac{1 + sT_2}{1 + sT_1} \qquad (5.10a)$$

$$where\ T_1 = (R_1 + R_2)C \qquad (5.10b)$$

$$and\ T_2 = R_2C \qquad (5.10c)$$

Substituting (5.10) into (5.4),

$$H(s) = \frac{s\omega_n(2\zeta - \omega_n/(K_0K_d)) + \omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \qquad (5.11a)$$

$$where\ \omega_n = (K/T_1)^{1/2} \qquad (5.11b)$$

$$and\ \zeta = 0.5(K/T_1)^{1/2}(T_2 + 1/K) \qquad (5.11c)$$

Hence, the addition of one zero to the filter allows the loop bandwidth and the loop gain K to be chosen (or ω_n) independently. The root locus and closed loop response are shown in Fig.5.6.

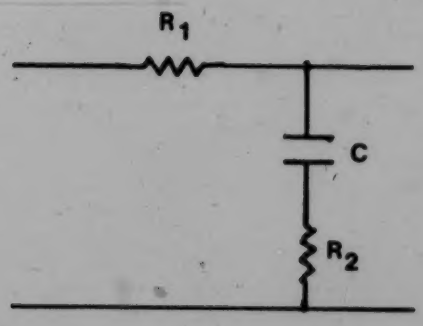
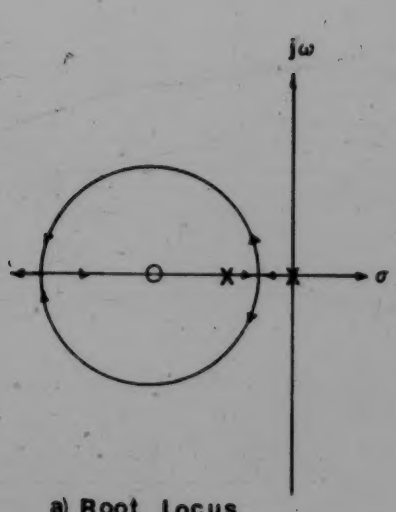
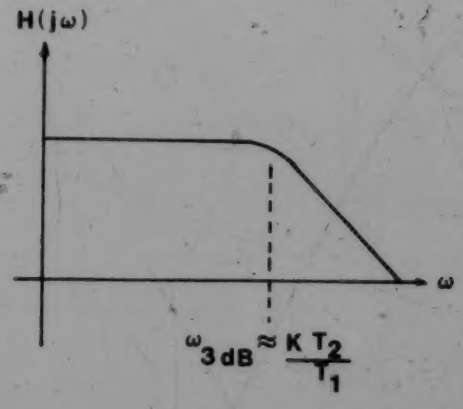


FIG. 5.5: A LAG-LEAD FILTER



a) Root Locus



b) Closed Loop Response

FIG.5.6: RESPONSES FOR A PLL WITH A LAG-LEAD FILTER

5.3 Linear Tracking

In this section, the steady state phase error θ_e that results from a specified input θ_i will be examined. The ability to achieve a small phase error is usually considered to be the criterion for good tracking performance. If the error should become so large that the PLL loses lock, cycle slipping will occur which, in a digital communication system will cause errors to be generated.

5.3.1 Steady State Error

Writing (5.5) explicitly in term of $\theta_e(s)$, we obtain

$$\theta_e(s) = \frac{s\theta_i(s)}{s + KF(s)} \qquad (5.12)$$

The steady state errors will be evaluated by means of the final value theorem of Laplace transforms, which states that

$$\lim_{t\to\infty} y(t) = \lim_{s\to 0} sY(s) \qquad (5.13)$$

$$\lim_{t\to\infty} \theta_e(t) = \lim_{s\to 0} \frac{s^2\theta_i(s)}{s + KF(s)} \qquad (5.14)$$

Consider the steady state error resulting from a step change of input phase of magnitude $\Delta\theta$. Then

$$\theta_i(s) = \Delta\theta/s \qquad (5.15)$$

Substituting (5.15) into (5.14),

$$\lim_{t\to\infty} \theta_e(t) = \lim_{s\to 0} \frac{s\Delta\theta}{s + KF(s)} = 0 \qquad (5.16)$$

Equation (5.16) shows that the loop will eventually track any change of input phase; there is no steady state error resulting from a step change of phase.

Next, consider the steady state error resulting from a step change of frequency of magnitude $\Delta\omega$. For this case the input phase is a ramp $\theta_i(t) = \Delta\omega t$,

$$\theta_i(s) = \Delta\omega/s^2 \qquad (5.17)$$

Substituting (5.17) into (5.14) yields

$$\theta_p = \lim_{t \to \infty} \theta_e(t) = \lim_{s \to 0} \frac{\Delta\omega}{s + KF(s)} = \frac{\Delta\omega}{KF(0)} \qquad (5.18)$$

The product KF(0) is often called the velocity constant or d.c. loop gain and is denoted by K_v . For a passive low pass filter,

$$F(0) = 1 \qquad (5.19)$$

$$K_v = K \qquad (5.20)$$

Equation (5.18) is useful when considering clock recovery, because there usually exist a difference in frequency between the PLL free running frequency and the signal pulse repetition rate. This difference constitutes $\Delta\omega$ of (5.18). Hence the phase error that results from this mistuning is given by (5.18) and (5.19):

$$\theta_p = \Delta\omega/K \qquad (5.21)$$

Thus for a given mistune, θ_p can be made as small as possible by increasing the loop gain K.

5.3.2 Transient Response

The steady state error of a PLL was given in the last section. This error is normally not a very important factor in clock recovery because this phase error can be offset by a phase shifter (or a time delay). What is more important to know is the transient behaviour of the PLL for a given input. It will be shown that, if the parameters of the PLL are not well chosen, then some ringing will occur during the transient response. A ringing transient response of a PLL used as a timing extraction process will be translated into timing jitter. This is undesirable, as mentioned in the last chapter, since in a chain of such regenerators the jitter will accumulate. This section will outline the transient response for a first- and for a second-order PLL; also, for a second-order PLL, the lag and lag-lead filters will be compared.

1) *First Order loop*

From (5.14) and (5.18), it can be shown that the transient response for a step phase input is

$$\theta_e(t) = \Delta\theta e^{-Kt} \qquad (5.22)$$

while that for a step frequency input is [47]

$$\theta_e(t) = \frac{\Delta\omega}{K}(1 - e^{-Kt}) \qquad (5.23)$$

where $\Delta\theta$ is the phase step, $\Delta\omega$ is the frequency step and K is the loop gain.

It can be seen that the loop gain K plays a major role in the transient response. A larger K would be desirable but, at the same time, the loop bandwidth would be greater (see (5.7a)) which is undesirable in terms of noise rejection. This problem can be overcome by the use of a high gain second order loop.

2) *Second-order Loop*

Two cases will be considered.

Using a simple filter with $F(s)=1/(1+T_1 s)$, then, from (5.5) and (5.9),

$$\frac{\theta_e(s)}{\theta_i(s)} = 1 - H(s) = \frac{s^2 + 2\zeta\omega_n s}{s^2 + 2\zeta\omega_n s + \omega_n^2} \qquad (5.24)$$

For a step phase, and from (5.15) and (5.24),

$$\theta_e(s) = \frac{(s + 2\zeta\omega_n)}{s^2 + 2\zeta\omega_n s + \omega_n^2} \qquad (5.25a)$$

$$where\ \omega_n = (K/T_1) \qquad (5.25b)$$

$$and\ \zeta = 0.5(1/(KT_1))^{1/2} \qquad (5.25c)$$

The time domain solution for (5.25a) is illustrated in Fig.5.7. For a step frequency input, the phase error can be determined from (5.17) and (5.24) to give

$$\theta_e(s) = \frac{\Delta\omega(s + 2\zeta\omega_n)}{s(s^2 + 2\zeta\omega_n s + \omega_n^2)} \qquad (5.26).$$

where again ω_n and ζ are given by (5.25b) and (5.25c) respectively. The corresponding time domain solution for (5.26) is given in Fig.5.8.

Another (or a second) possibility is to use a filter with a transfer characteristic $F(s)=(1+T_2s)/(1+T_1s)$. From (5.5),(5.11), and (5.15), the phase error for a step phase input is

$$\theta_e(s) = \frac{(s + \omega_n^2/K)\Delta\theta}{s^2 + 2\zeta\omega_n s + \omega_n^2} \qquad (5.27a)$$

$$where\ \omega_n = (K/T_1)^{1/2} \qquad (5.27b)$$

$$and\ \zeta = 0.5(K/T_1)^{1/2}(T_2 + 1/K) \qquad (5.27c)$$

Fig.5.9 illustrates an approximate time domain response of (5.27), for very large K, which is actually meant for a loop with an ideal integrator.

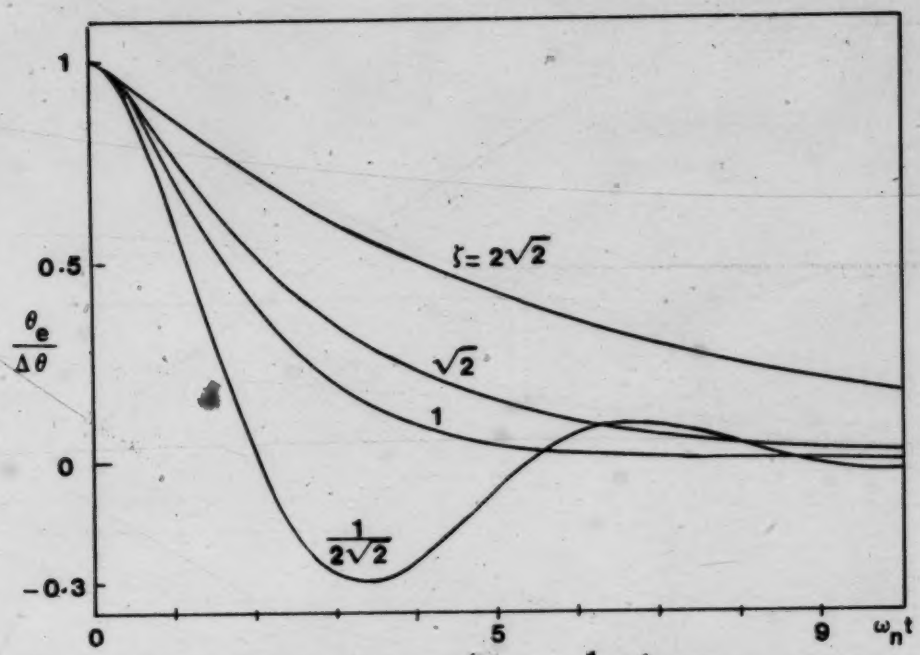


FIG.5.7: SECOND-ORDER LOOP $\left\{F(s) = \frac{1}{1 + T_1 s}\right\}$; PHASE ERROR FOR A STEP PHASE OF THE INPUT SIGNAL

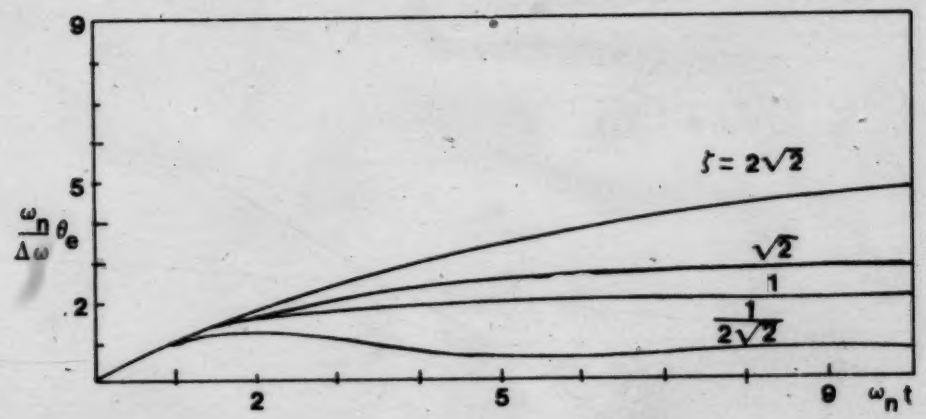


FIG.5.8: SECOND-ORDER LOOP $\left\{F(s) = \frac{1}{1 + T_1 s}\right\}$; PHASE ERROR FOR A STEP FREQUENCY OF THE INPUT SIGNAL

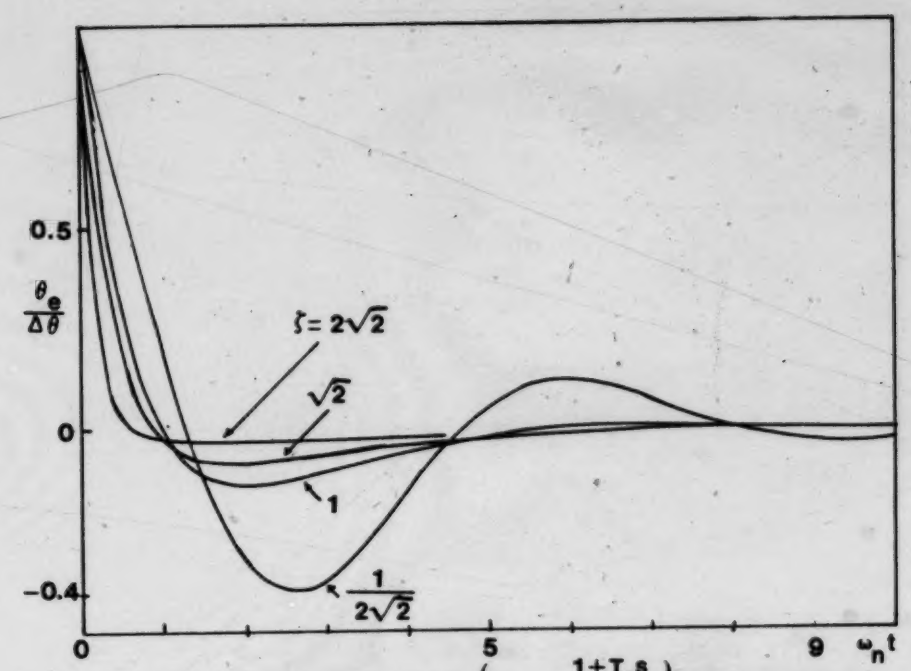


FIG. 5.9: SECOND-ORDER LOOP $\left\{F(s)=\frac{1+T_2 s}{T_1 s}\right\}$; PHASE ERROR FOR A STEP PHASE OF THE INPUT SIGNAL.

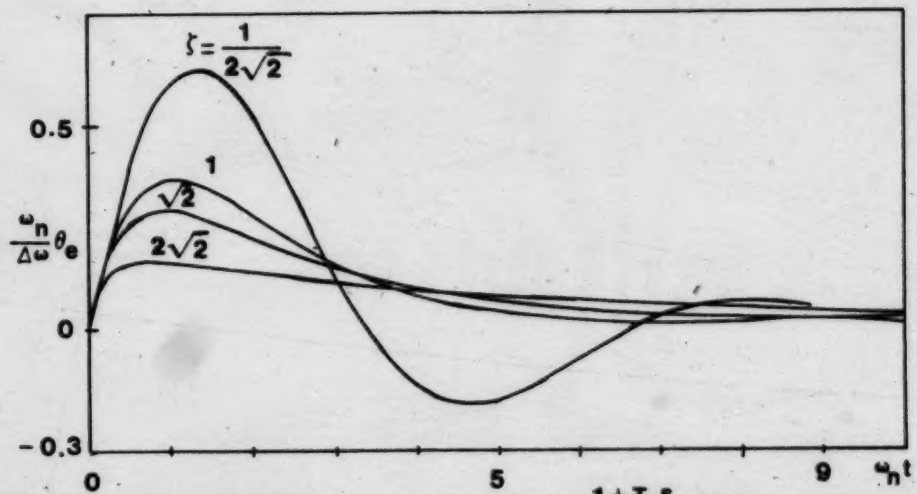


FIG. 5.10: SECOND-ORDER LOOP $\left\{F(s)=\frac{1+T_2 s}{T_1 s}\right\}$; PHASE ERROR FOR A STEP FREQUENCY OF THE INPUT SIGNAL

The same procedure can be carried out for a step frequency input. From (5.5),(5.11),and (5.17), the phase error is given by

$$\theta_e(s) = \frac{\Delta\omega}{s^2 + 2\zeta\omega_n s + \omega_n^2} + \frac{\omega_n^2}{K}\,\frac{\Delta\omega}{s(s^2 + 2\zeta\omega_n s + \omega_n^2)} \qquad (5.28)$$

where ω_n and ζ are defined by (5.27b) and (5.27c), respectively.

The solutions of (5.28) as given by Blanchard[47] are:

$$\text{For } \zeta<1,\ \theta_e(t) = \frac{\Delta\omega}{K} + \frac{\Delta\omega}{\omega_n} e^{-\zeta\omega_n t}$$

$$\left[\frac{1 - \omega_n/K}{\zeta^2 - 1}\sinh \omega_n(\zeta^2 - 1)^{1/2}t - \frac{\omega_n}{K}\cosh \omega_n(\zeta^2 - 1)^{1/2}t\right]$$

$$\text{For } \zeta=1,\ \theta_e(t) = \frac{\Delta\omega}{K} + \frac{\Delta\omega}{K} e^{-\omega_n t}(\omega_n t - \omega_n^2 t/K - \omega_n/K)$$

$$\text{For } \zeta>1,\ \theta_e(t) = \frac{\Delta\omega}{K} + \frac{\Delta\omega}{K} e^{-\zeta\omega_n t}$$

$$\left[\frac{1 - \omega_n/K}{1 - \zeta^2}\sin \omega_n(1 - \zeta^2)^{1/2}t - \frac{\omega_n}{K}\cos \omega_n(1 - \zeta^2)^{1/2}t\right] \qquad (5.29c)$$

The time domain responses for (5.29) are shown in Fig.5.10. These responses are exact only for very large K and for the static phase error $\Delta\omega/K$ assumed negligible.

Results have been shown so far for second-order loops with lag and lag-lead filters. In both cases, for a step frequency input, the steady state phase error is given by $\Delta\omega/K$. This implies that a high value for K will reduce the static phase error. Unfortunately, for the PLL with a lag filter, increasing K results in a reduced loop damping factor (see (5.25c)). This is demonstrated clearly in Fig.5.8 where the static phase error which is inversely proportional to

K, increases with the damping factor ζ . A low value of ζ results in marked overshoot and relative instability of the loop. The use of lag-lead filter will to some extent overcome this problem. A high loop gain can be chosen fairly independently for the damping factor ζ (see (5.27b) and (5.27c)). In fact, for very large values of K, the second-order loop would resemble a loop with an ideal integrator which implies a zero static phase error for a step frequency input. Fig.5.10 shows responses for a second-order loop with an ideal integrator.

In summary, the high gain PLL with a lag-lead filter is one possible way to achieve a small static phase error, while at the same time giving a fast response without serious ringing. These properties are needed in the clock recovery process because the signal might have a long interval with no transitions (no timing information). At the next transition (or when the signal resumed) the PLL should have the ability to track this abrupt transition in the shortest possible time without any serious ringing in its response. The high gain of the PLL is necessary in order to achieve low sensitivity of the static phase error caused by any mistune of the PLL free-running frequency.

5.3.3 Steady State Response to a Ramp Frequency Input

Consider the input frequency is linearly changing with time at a rate of $\Delta\dot{\omega}$ rad/sec^2, that is

$$\theta_i(t) = \frac{1}{2}\Delta\dot{\omega}t^2 \qquad (5.30)$$

$$\theta_i(t) = \frac{\Delta\dot{\omega}}{s^3} \qquad (5.31)$$

If the loop gain K is finite, then, from (5.21) the phase error will grow without limit. Suppose K is made large enough that the static phase error is negiligible for the largest frequency change to be accomodated. From (5.5) and (5.11),

$$\frac{\theta_e(t)}{\theta_i(t)} = \frac{s^2 + s\omega_n^2/K}{s^2 + 2\zeta\omega_n s + \omega_n^2} \qquad (5.32)$$

$$\approx \frac{s^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \quad for\ K>>\omega_n^2 \qquad (5.33)$$

From (5.13) and (5.31),

$$\lim_{t\to\infty} \theta_e(t) = \lim_{s\to 0} \frac{\dot{\Delta\omega}}{s^2 + 2\zeta\omega_n s + \omega_n^2} \qquad (5.34)$$

$$\theta_e(t) = \frac{\dot{\Delta\omega}}{\omega_n^2} \qquad (5.35)$$

Equation (5.35) implies that, for a given rate of change of frequency, the dynamic phase error can be reduced by increasing the natural angular frequency ω_n. Unfortunately, as will be shown in the next section, the noise loop bandwidth is directly related to ω_n. The larger ω_n, the wider will be the noise bandwidth and the lower will be the noise rejection factor.

5.4 Noise Bandwidth

One of the major functions of a PLL is to reduce the noise in the reconstructed signal, in this case the clock signal. For simplicity, consider the system noise to be white and Gaussian, as will be discussed in Chapter 6. Since most of the noise at the output is usually restricted to a narrow band by the filtering action of the circuit, it is convenient to express the noise that remains as the bandwidth of an ideal filter (that is, a brick wall filter), that would pass the same mean square noise. The derivation of the noise bandwidth could be outlined as followed[48]:

Assume that the noise input to a filter of transfer function $H(j\omega)$ has a spectrum which is white. Then,

$$\overline{n_o^2} = N_o \int_0^\infty |H(j\omega)|^2 \, df \qquad (5.36)$$

where N_o is the one sided noise power spectral density.

There is an equivalent ideal rectangular filter, with a constant magnitude of H_R, and a bandwidth of B_n (hertz), such that the variance of the outputs of the two filters is equal if the white noise inputs are of equal density, that is,

$$\overline{n_o^2} = N_o H_R^2 B_n \qquad (5.37)$$

$$If\ we\ let\ H_R = H(0) \qquad (5.38)$$

where H(0) is the magnitude of the transfer function of the filter at zero frequency, then

$$B_n = \frac{\int_0^\infty |H(j\omega)|^2\, df}{|H(0)|^2} \qquad (5.39)$$

The noise bandwidth as given by Blanchard[48] for a second-order PLL with lag-lead filter is

$$B_n = \frac{\omega_n}{8\zeta}\left\{1 + \left(2\zeta - \frac{\omega_n}{K}\right)^2\right\} \qquad (5.40)$$

$$= \frac{\omega_n}{8\zeta}(1 + 4\zeta^2) \qquad for\ K >> \omega_n \qquad (5.41)$$

5.5 Locking Limits

The loop locking range is that range of input frequencies about the free-running frequency for which the loop maintains lock. In most cases, the loop locking range is bounded by the limited phase comparison range of the phase detector. The transfer chracteristic of a phase detector will depend on its circuit design as well as on the input waveforms[49]. In this project, a monolithic PLL was used in which a Gilbert cell analog multiplier[50] was being employed as its phase detector.

The Gilbert cell analog multiplier behaves like a sinusoidal phase detector when the inputs signals are both sinusoidal. On the other hand, if the inputs are square waveforms, then it behaves like a triangular phase detector[49]. As all our derived signals are digital, we would only be interested in the triangular phase detector. The characteristics of a triangular phase detector are shown in Fig.5.11.

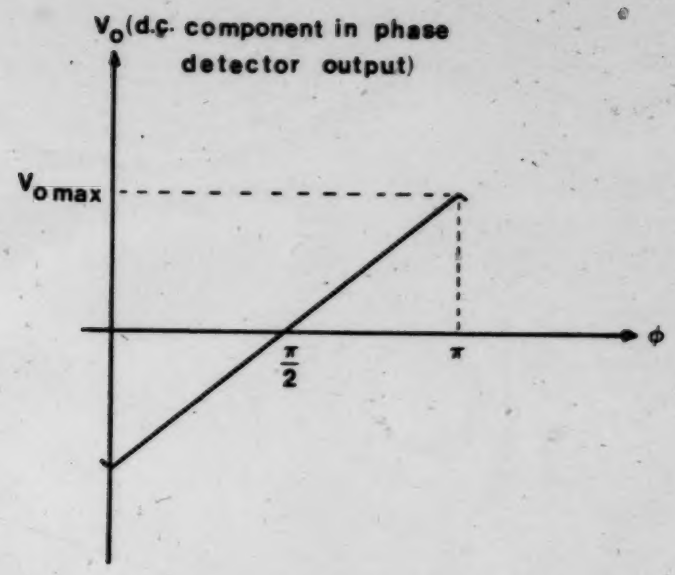


FIG. 5.11: VOLTAGE OUTPUT VERSUS PHASE DIFFERENCE OF A TRIANGULAR PHASE DETECTOR

In order for the PLL to maintain lock, the phase difference between the VCO output and the incoming signal must be kept between zero and π radian. The maximum voltage from the phase detector is

$$\bar{V}_{max} = \pm K_d(\pi/2) \qquad (5.42)$$

where K_d is the phase detector conversion gain.

This d.c. voltage is applied to the VCO input, producing a frequency shift from its free-running frequency. From (5.21), the maximum deviation in frequency is given by

$$\Delta\omega_{osc} = K_d K_0(\pi/2) = K\pi/2 \qquad (5.43)$$

If the input frequency is shifted further away from the free running frequency, more voltage would have to be applied to the VCO in order for the VCO frequency to shift accordingly. However, the phase detector can produce no more d.c. output voltage to shift the VCO frequency further. This results in the loop losing its lock. The locking range $\Delta\omega_L$ is then

given by

$$\Delta\omega_{osc\ max.} = \Delta\omega_L = K\pi/2 \qquad (5.44)$$

Incidentally the locking range for a sinusoidal phase detector, is $\Delta\omega_L = K$,and for a sawtooth phase detector, $\Delta\omega_L = \pi K$.

Equation (5.44) gives the frequency range on either side of the free running frequency for which the loop will track the input frequency variation. It is a parameter that depends only on the d.c. gain in the loop and on the phase detector characteristics. It is independent of the properties of the loop filter[51]. The dynamic error in a second-order loop was given in (5.35), from which the maximum permissible rate of change of the input frequency for a a triangular phase detector can be deduced to give

$$\dot{\Delta\omega} = \omega_n^2\pi/2 \qquad (5.45)$$

For a sinusoidal phase detector it is

$$\dot{\Delta\omega} = \omega_n^2 \qquad (5.46)$$

And for a sawtooth phase detector it is

$$\dot{\Delta\omega} = \pi\omega_n^2 \qquad (5.47)$$

Among these three phase detectors, the sawtooth phase detector offers the largest permissible rate of change of input frequency. The sawtooth phase detector is designed with flip flops and hence it has memory. As a result, a missing transition of the input signal will cause a very large error to appear for a short time. This is undesirable as far as timing extraction is concerned[52].

5.6 Seize Frequency

The seize frequency is defined as the maximum mistuning of a suddenly connected signal that cannot cause a discontinuity after the initial phase jump.

It was mentioned earlier that a multiplier phase detector will produce a zero signal when there is no input signal. With such a device, the effect of suddenly applying a signal can be interpreted to be similar to a step phase shift of an arbitrary value between $-\pi/2$ and $\pi/2$ (for triangular phase detector) and a step change in frequency equal to the mistuning of the signal $\Delta\omega$. Seize frequency can therefore be explained as the maximum mistuning of the signal, which when suddenly applied, will allow the PLL to lock onto the signal without exhibiting any discontinuities in its phase error (output of the phase detector). For the clock recovery process, it is vital that the PLL circuit lock immediately onto the suddenly applied signal without discontinuities of the phase error, which will otherwise result in great uncertainty in the phase of the regenerated clock signal.

For a high gain second-order PLL with a lag-lead filter, the seize frequency for the triangular phase detector is given by Byrne [53] as

$$\omega_s = \frac{T_2}{T_1} \quad (lock\ frequency) \tag{5.48}$$

$$Hence,\ \omega_s = \frac{\pi}{2} K \frac{T_2}{T_1} \tag{5.49}$$

From (5.27b),

$$Therefore,\ \omega_s = \frac{\pi}{2} \omega_n^2 T_2 \tag{5.50}$$

Hence the seize frequency is proportional to the square of the natural angular frequency of the loop.

In this chapter, some basic concepts and principles of PLLs have been discussed. In a high gain second-order PLL, the loop response and noise bandwidth can be adjusted independently, which will be shown to be useful in the next chapter, where the optimization of the PLL parameters for clock extraction is considered in detail.

Chapter 6

CLOCK RECOVERY FOR A 4-LEVEL PWM SYSTEM

A 4-level PWM system was earlier shown (see Chapter 3) to achieve a BER of 10^{-9} at a received optical power of approximately 1 nW. However, the system performance was measured on the basis that the timing reference was obtained from a master clock. It will be shown that a 4-level PWM system with a self-recovered clock can give a BER performance comparable to that using ideal timing (that is, the master clock).

Like any conventional digital communication system, in order to restrict the phase jitter of the recovered clock or timing signal, the timing extraction circuit needs to be carefully designed. For the work here, a second-order PLL with a lag-lead filter was used as the timing extraction device. The characteristics of the PLL as a timing extraction device will depend largely on the chosen values of its various parameters, such as ω_n , ζ and K.

This chapter begins with a comparison of the relative strength of the line spectrum at the pulse repetition frequency of a 4-level PWM signals with binary RZ and NRZ code formats. It goes on to discuss the sources of clock jitter, with particular reference to a PWM optical fiber system which has an additional source of noise - the shot noise. However, no attempt has been made to quantify these types of jitter; they are discussed qualitatively only, since a mathematical analysis requires a great deal of statistical analysis[54,55,56]. Following this, some general principles of optimization are outlined and these principles are related to the optimization of PLL performance in clock recovery. In the final part of this chapter, experimental results of the system BER perfomance as a function of the various values of the PLL paramters are presented. The results show the range of optimised values of noise bandwidth, damping factor, and loop gain for which the system BER performance is comparable to that using a master clock.

6.1 Timing Extraction for a 4-level PWM System

6.1.1 Timing Content of a 4-level PWM Signal

The merits of a PWM signal with regard to timing extraction have been discussed in Chapter 4. In a 4-level PWM signal, three out of the four codes or symbols have pulses of

definite width. That is, with the exception of the t_0 pulse, the t_1, t_2 and t_3 pulses are 100ns, 200ns and 300ns wide, respectively. These pulses have a positive rising edge which may be used to trigger a one-shot monostable circuit, producing pulses of consistent width. If the 4-level PWM signal is truly random, the three out of every four symbols will have positive rising edges and, therefore, the probability of having a pulse (for a given pulse interval) at the output of the monostable is 0.75. This is higher than the binary RZ code format where the probability of having a pulse in a given time slot is 0.5. For the binary NZR code format which depends only on the positive rising edge of each pulse to trigger the monostable, the probability is only 0.25. The strength of the line spectrum at the fundamental pulse repetition frequency can be computed by the autocorrelation technique (see Appendix B). The line spectral voltage of the above 3 code formats at the fundamental pulse repetition frequency, is :

$$\textit{4-level PWM:} \quad v = \frac{3E}{4\pi} \sin\left(\frac{\pi t_o}{T}\right) \tag{6.1a}$$

$$\textit{Binary RZ code format:} \quad v = \frac{E}{2\pi} \sin\left(\frac{\pi t_o}{T}\right) \tag{6.1b}$$

$$\textit{Binary NRZ code format:} \quad v = \frac{E}{4\pi} \sin\left(\frac{\pi t_o}{T}\right) \tag{6.1c}$$

It is clear from the above comparison that a PWM signal has the strongest timing content.

6.1.2 Sources of Timing Jitter

Sources of timing jitter in an optical fiber communication system are:

1) Thermal and shot noise at the receiver
2) Channel imperfection
3) Intersymbol interference
4) Mistuning of the PLL free running frequency
5) Instability of the transmitter clock

The slope theory discussed in Chapter 2 may however be used to determine the relationship between timing jitter and system noise. The phase shift can be related to the noise voltage by

$$\tau_n = \frac{\sigma_T}{s'} \qquad (6.2)$$

where, from (2.10), $\sigma_T^2 = \sigma_{th}^2 + (\sigma_m^2 - \sigma_{th}^2)V_0(t)_s/V_{max}$

and s' is the slope of an ideal PWM waveform which is determined by the system bandwidth (see Fig. 6.1). Since σ_T is signal dependent, τ_n is to some degree also signal dependent. Another signal dependent contribution to τ_n, but perhaps less significant, is the intersymbol interference(I.S.I.) effect. I.S.I. will result in some displacement of the positive rising edges of the PWM signal.

Mistuning of the PLL free runing frequency with respect to the pulse repetition frequency of the signal is perhaps one of the most important sources of timing jitter. If there is a long run of data with transitions, then the PLL will be able to track and update its phase continuously. At the other extreme, if there is a long run of data without a transition, then no timing information is supplied to the loop for the duration of such a run. Consequently, the phase of the VCO will drift away from its correct position. Ideally one would tune the free running frequency to be equal to the pulse repetition frequency, but drift is inevitable due to external noise and circuit parameter changes with power supply fluctuations, temperature, humidity and/or time.

The resulting PWM signal after the monostable circuit can ideally be approximated by [57]

$$\gamma(t) = \sum_{n=0}^{N} c_n \delta(t - nT - \tau_n) \qquad (6.3)$$

where the coefficient c_n can be determined from the statistical properties of the signal, that is the timing content of the original signal; c_n can take the binary value of '1' or '0'; T is the pulse repetition interval and τ_n is defined in (6.2).

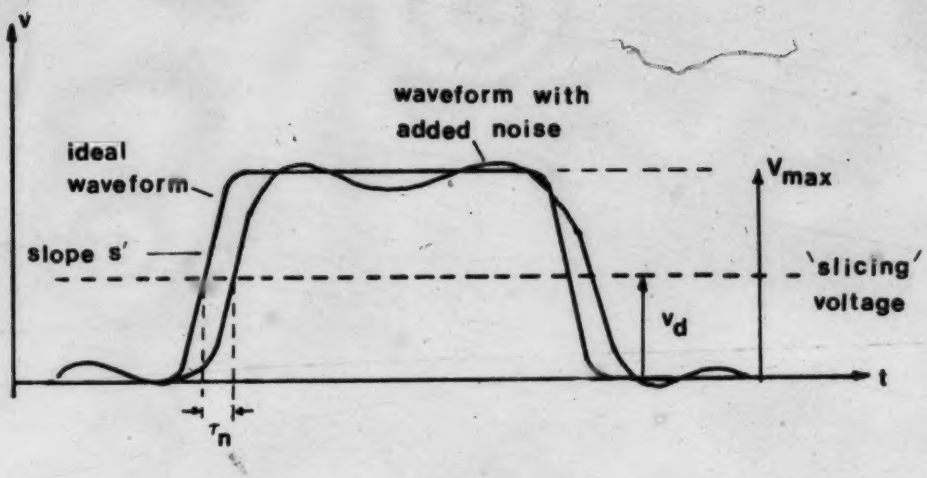


FIG. 6.1: PHASE SHIFTING OF THE RISING POSITIVE EDGE

6.1.3 Optimizing PLL Performance in Clock Extraction

1)*Choosing the Type of PLL to be used*

Chapter 5 discussed various possible configurations of the PLL. In summary, the high gain second-order PLL with lag-lead filter was favoured because:

1)For a given amount of mistuning of the PLL and during the period of the signal experiencing a long run of zeros, the PLL will tend to drift towards its free running frequency. A signal with a long run of zeros, suddenly followed by signal transitions is seen by the mistuned PLL to be similar to a step frequency change at the input(assumed to be within the seize frequency range). For a second-order PLL with very high loop gain, this mistuning problem will not give rise to significant static phase error.

2)A second order loop has a low pass characteristic which attenuates fast changing phase errors due to noise in the input signal. This cannot be achieved by the first order loop because the narrower bandwidth would mean lower loop gain K, which implies poor tracking capability.

3)A PLL with a lag-lead filter has the flexibility of allowing adjustment of the three loop parameters, the natural angular frequency, the damping factor, and the loop gain

independently. It could be designed with a large K yet, at the same time, not suffer from underdamped behaviour. The price for this flexibility is a somewhat more complicated design procedure and a bit more circuitry.

2)*General Principles of Optimization*

Chapter 5 discussed the effect of the loop bandwidth (or the noise bandwidth) on the PLL performance. A narrow bandwidth will minimise output phase jitter, while a wide bandwidth will minimise the transient error to obtain the best tracking and acquisition properties. Both the output phase jitter and transient error will contribute to the overall jitter of the recovered clock signal. Improvement in one can be achieved only at the expense of the other, and therefore some compromise or optimization is necessary.

A well known optimization principle has been derived by Jaffe and Rechtin[58]. They state that the mean square loop error is given by:

$$\Sigma\theta^2 = \overline{\theta_{n_0}^2} + \lambda^2 E_T^2 \qquad (6.4)$$

where θ_{n_0} is the phase jitter due to interference and E_T^2 is a measure of the total transient error given by

$$E_T^2 = \int_0^\infty \theta_e^2(t)dt \qquad (6.5)$$

where $\theta_e(t)$ is the instantaneous phase error in the loop due to transients. The quantity λ is a multiplier that establishes the relative proportions of noise and transient error that are to be permitted.

3)*PLL Parameters Optimization*

Three of the most important PLL parameters applicable to clock recovery are the loop gain, the noise bandwidth, and the damping factor. As theoretical optimization of these parameters is complex and beyond the scope of this thesis, attempts were only made to determine the optimum values experimentally. Nevertheless, in the following we will briefly discuss how the proper choice of parameters helps to reduce timing jitter.

For a VCO whose free running frequency fluctuates with temperature, moisture and time, a high gain PLL will help to reduce any static phase error that may arise from this mistuning. If a low-gain loop is to be used, then a highly stable VCO must be employed[42]. From a cost point of view, it is still more economical to obtain a monolithic PLL with high gain than a highly stable VCO.

The major function of the PLL is the extraction of a signal immersed in noise. This requires a narrow noise bandwidth. The relation between output jitter and input jitter is largely dependent on the noise bandwidth of the loop. In other words, for a given jitter input, the smaller ω_n (hence noise bandwidth), the smaller will be the output time jitter. Unfortunately there is a limit because the transient response is also related to ω_n, but in the opposite direction.

When a PLL is designed from the specifications of jitter accumulation, ζ must be as large as possible for a given noise bandwidth[6.6]. Unfortunately, if the noise bandwidth is kept constant, ω_n must decrease when ζ is increased, hence again the transient response time becomes larger[42].

6.2 Experimental Configuration for Clock Recovery System

A complete 4-level PWM system with self generating clock was designed, built and tested in the laboratory. A major objective of this work was to determine experimentally the relationship between the various PLL parameters such as loop gain, noise bandwidth and damping factor, and the timing jitter. To measure directly the magnitude of timing jitter would require a jitter measuring instrument which would be costly to purchase. As there is a direct relation between system BER and the jitter of the recovered clock signal, the more practical alternative is therefore to measure the system BER when each of the three PLL parameters is varied while the other two are kept constant. In other words, it can be assumed that as the timing jitter (clock jitter) increases, BER will increase and vice versa. Hence, by maintaining constant the values for all system parameters, except the one of interest, any change in system BER performance can be interpreted to be a change in the magnitude of the timing jitter caused by that single parameter variation. To achieve the objective of PLL parameter optimization, the following measurements were made:

1) BER as a function of the PLL noise bandwidth,

2) BER as a function of the PLL damping factor,

3) BER as a function of mistuning of the PLL, for various loop gains.

4) BER as a function of received optical power, for various values of the loop parameters.

5) Timing jitter as a function of data pattern.

6.2.1 Overall Experimental Setup

The overall experimental setup is the same as in Chapter 3, with the exception that the timing reference is now taken from the timing extracting circuit rather than from the master clock.

6.2.2 The Timing Extraction Circuit

The block diagram of the timing extraction circuit is shown in Fig.6.2. The detailed circuit diagram can be found in Fig.3.3. and Fig.6.3.

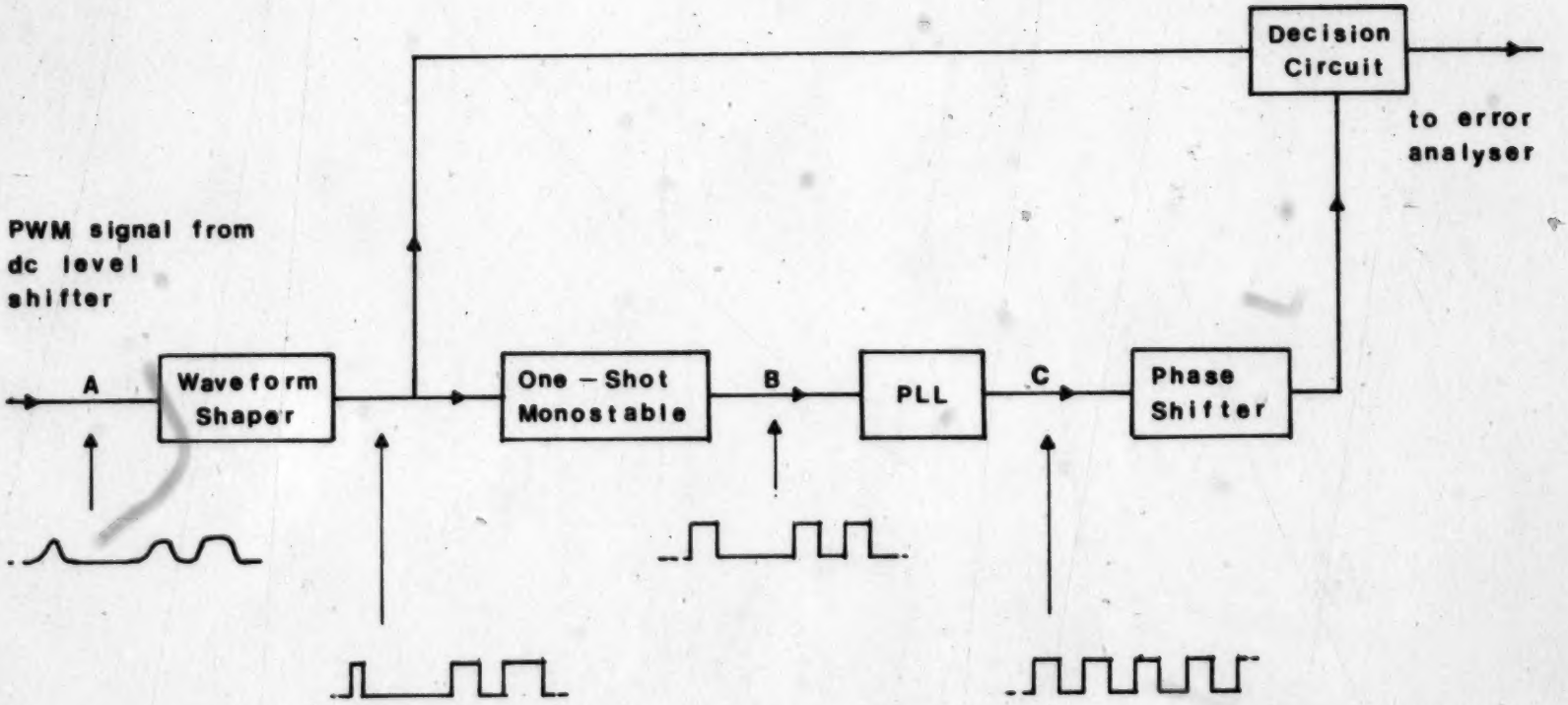
The timing extraction is taken right after the waveform shaper, in which the PWM waveforms are reshaped into a rectangular format of various widths. The one-shot monostable then produces a pulse train of consistent width ($t_o = T/2$) from the positive rising edge of the rectangular waveforms. The pulse train from the monostable is then used to stimulate the PLL, to produce a continuous pulse train of the same frequency. The phase shifter functions as a time delay to enable the extracted clock to be properly synchronized with the data signal. It is made up of two one-shot monostables circuits connected in series, one of which triggers on the positive rising edge and the other on the negative falling edge. By adjusting the width of the pulse produced by the first monostable, a delay in time can be introduced. In the following, we will take a detailed look at the PLL, as it is the most important device in the whole experiment.

The XR215 (made by EXAR company) is a monolithic PLL which can be operated up to 30MHz. It is a low cost, general purpose PLL. A schematic of the PLL and the required external connections is shown in Fig.6.3.

The filters connected at pin 2 and pin 3 are lag-lead filters, with R_1 (6000 ohms) being internally connected to the phase detector at pin 2 and pin 3.

The VCO free running frequency f_R is determined by selection of C_0 across pins 13 and 14 and can be finely tuned by connecting an external resistor R_x between pin 10 and ground. It can be approximated as

$$f_R = \frac{200}{C_0}\,(1 + 0.6/R_x) \qquad (6.6)$$



FIG·6.2 : Schematic of a Timing Extraction Circuit

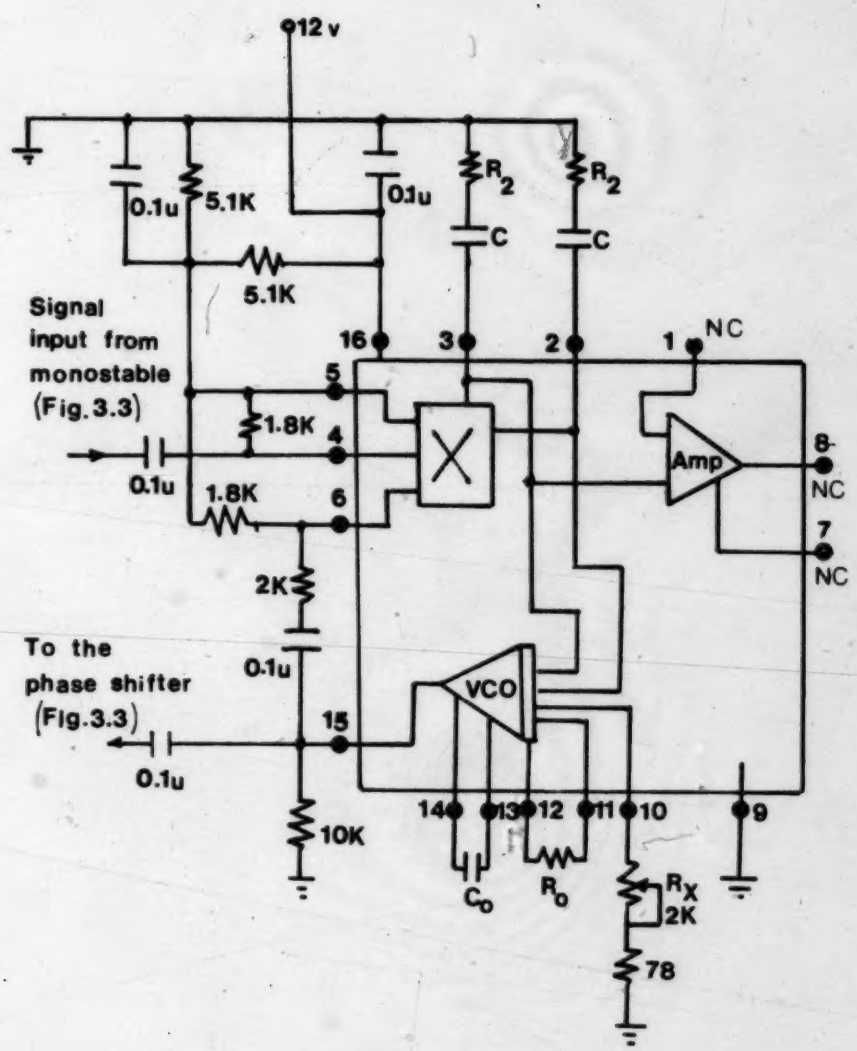


FIG.6.3: THE PLL (XR 215) AND ITS EXTERNAL CONNECTIONS

where C_o is in uF and R_x is in $K\Omega$.

The phase comparator gain K_d is given as K_d =2 volt/rad if the input signal voltage exceeds 50mV rms.

The VCO conversion gain K_o is determined by the choice of the timing capacitor C_o and the gain control resistor R_o, connected externally across pins 11 and 12. It is given by

$$K_0 = \frac{700}{C_0 R_0} \quad (rad/sec)/volt \qquad (6.7)$$

where C_o is in uF and R_o is in $K\Omega$.

In the experiments, the 3 major PLL parameters varied were the natural angular frequency ω_n , loop gain K, and the damping factor ζ ; ω_n and ζ are chiefly determined by the characteristic of the filter, while the loop gain $K = K_0 K_d$ rad/sec.

$$K = \frac{2 \times 700}{C_0 R_0} \quad rad/sec \qquad (6.8)$$

From (5.11b) and (5.11c),

$$\omega_n = (K/T_1)^{1/2} = (K\omega_1)^{1/2} \qquad (6.9a)$$

$$where\ \omega_1 = \frac{1}{T_1} = \frac{1}{(R_1 + R_2)C} \qquad (6.9b)$$

$$\zeta = \frac{1}{2}\omega_n\left(\frac{1}{\omega_2} + \frac{1}{K}\right) \qquad (6.10a)$$

$$where\ \omega_2 = 1/T_2 = 1/(R_2 C) \qquad (6.10b)$$

Dividing (6.9b) by (6.10b),

$$\frac{\omega_1}{\omega_2} = \frac{R_2}{R_1 + R_2} = \frac{R_2}{6000 + R_2} \qquad (6.11)$$

Further rewriting (6.9a) and (6.10a) explicitly in terms of ω_1 and ω_2, respectively,

$$\omega_1 = \frac{\omega_n^2}{K} \qquad (6.12)$$

and

$$\omega_2 = \frac{K\omega_n}{2\zeta K - \omega_n} \qquad (6.13)$$

For $\zeta K >> \omega_n$, (6.13) becomes

$$\omega_2 \simeq \frac{\omega_n}{2\zeta} \qquad (6.14)$$

which is independent of K.

At this point, a numerical example to show how the component values are obtained will be given.

Consider the following PLL parameter values:

$K = 1 \times 10^6$ rad/sec,

$\omega_n = 0.1 \times 10^6$ rad/sec

$\zeta = 1.0$,

Using (6.8), if $C_0 = 220pF$

then $R_0 \simeq 6.36\ K\Omega$

For $\omega_n = 0.1 \times 10^6$ rad/sec, and from (6.12),

$\omega_1 = 10^4$ rad/sec.

If $\zeta = 1.0$, from (6.13),

$\omega_2 = 5.2 \times 10^4$ rad/sec

Therefore $\frac{\omega_1}{\omega_2} = 0.192$

Using (6.11),

$R_2 = 1.5\ K\Omega$

Since $\omega_2 = 1/(R_2C)$

Therefore $C = \dfrac{1}{5.2\text{x}10^4\text{x}1.5\text{x}10^3}$

$= 12.8\ nF$

Hence, for the given PLL parameters values, a second-order PLL with lag-lead filter can be readily designed.

In the following section, the results are given for different values of the three parameters; To study the effect of each of these parameters on the BER performance of the system, one of these parameters was varied while the other two, including all other system parameters were kept constant.

6.2.3 Measurement Result

Experiments for BER vs. noise bandwidth, BER vs. damping factor and BER vs. mistuning of the PLL frequency, all. employed a pseudo-random signal of $10^{20}-1$ bit length. This pseudo-random signal is used in order to simulate the randomness of an actual message signal. For all these 3 experiments, the received optical power was maintained at approximately 1 nW.

1) *Noise Bandwidth vs. BER*

In this part of the experiment, the effect on BER of a changing noise bandwidth was studied. In (5.41), an expression for the noise bandwidth was given whose derivation was based on the assumption that the input noise is white and Gaussian. For the system used in this experiment, there is both shot noise and thermal noise but, as discussed in Chapter 3, the shot noise can be approximated as being Gaussian. Hence, the sum of both the shot noise and the thermal noise can be approximated by a Gaussian distribution. As the maximum noise

bandwidth of the PLL being used in this experiment was 6250Hz, which is a small compared to the system bandwidth (5MHz), the system noise can be assumed to be white.

In order to reduce the static phase error, K must be large and in this case we use K=1x10⁶ rad/sec. If $K >> \omega_n$, then (5.41) becomes,

$$\omega_n = \frac{8\zeta B_n}{1 + 4\zeta^2} \qquad (6.15)$$

There is another variable to consider, and that is the damping factor ζ. Here, $\zeta = 1.0$ was chosen because this will not cause the closed loop performance to be underdamped nor overdamped, that is, it is critically damped. Hence, what is left is the natural angular frequency ω_n. By changing ω_n, the noise bandwidth will be varied accordingly. Fig.6.4 shows the experimentally observed BER as a function of the product of noise bandwidth and pulse repetition interval(T). As an example of the design procedure, assume the PLL values to be:

$B_n = 6250$ Hz,

$K = 1x10^6$ rad/sec

$\zeta = 1.0$,

From (6.15),

$$\omega_n = \frac{8 \times 6250}{5} = 1x10^4 \text{ rad/sec.}$$

Going through the same procedures as in the last example,

$R_0 = 6.36$ KΩ (for $C_0 = 220$pF)

$\omega_1 = 100$ rad/sec, $\omega_2 = 5200$ rad/sec , $\frac{\omega_1}{\omega_2} = 0.019$

Therefore, $R_2 = 120\Omega$ and $C = 1.6$uF

It was found experimentally that for B_nT smaller than 0.0005, any slight mistuning of the PLL will cause cycle slipping and hence the collapse of the system. Similarly,

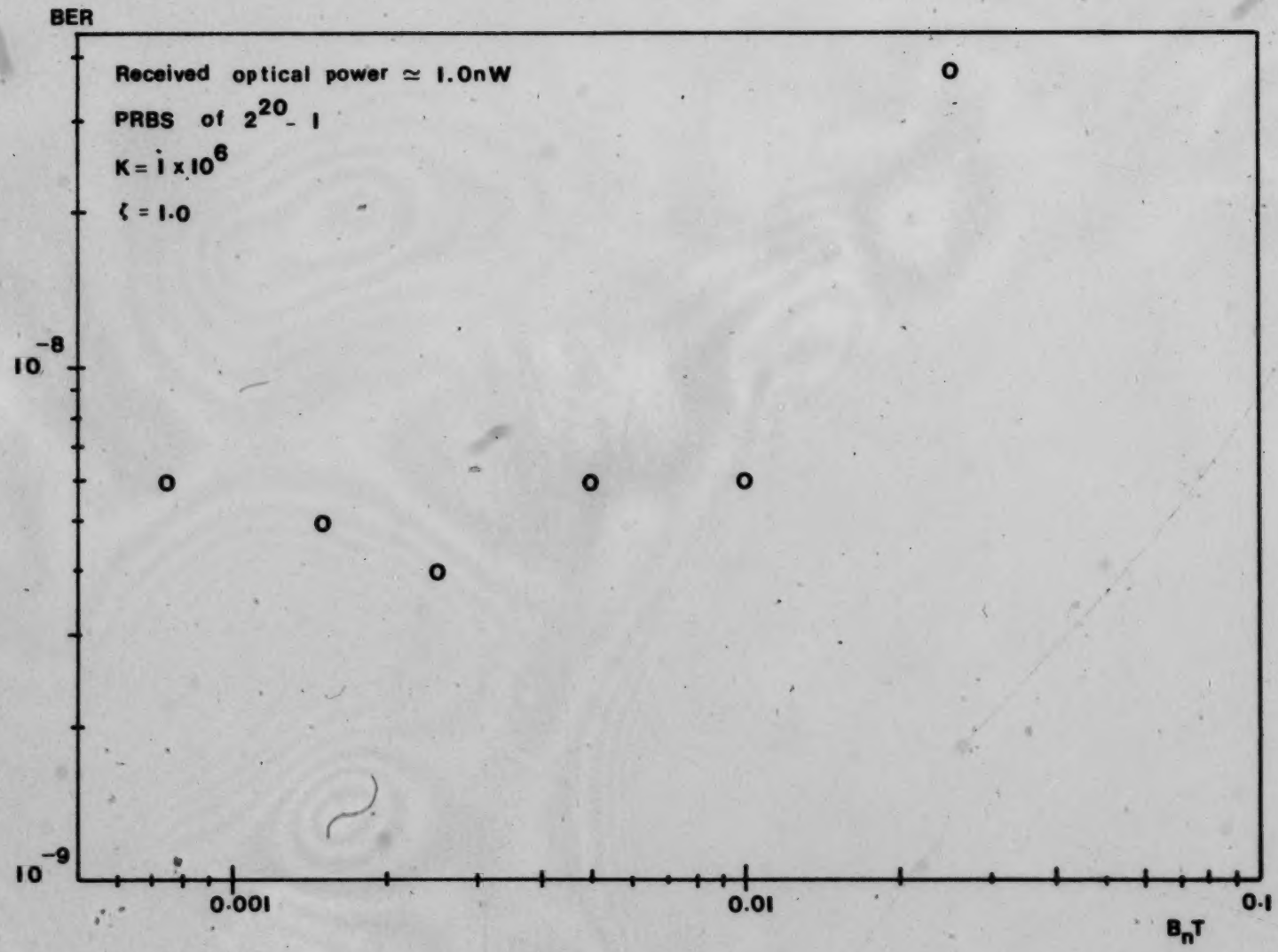


FIG.6.4 : BER vs Product of Noise Bandwidth and Time Period

BER will suffer greatly when B_nT is greater than 0.01.

2) *Damping Factor vs. BER*

This part of the experiment examines how sensitive the BER is to the damping factor. (or vice-versa). In order to make this measurement, it is necessary to keep the noise bandwidth constant for various values of ζ in order to maintain the same degree of interference from external noise. Again we used a high loop gain, K=1x10^6 rad/sec.

Assuming the noise bandwidth B_n = 6250Hz, therefore ω_n can be obtained for any value of ζ (see (5.15)). The calculation of R_0, R_2 and C can be done using the same procedures as in previous examples. Experimental results of BER vs. various values of ζ are presented in Fig.6.5. It shows that the damping factor is not a strong function of BER as long as the damping factor is not smaller than 0.25.

3) *BER vs. Mistuning of PLL Frequency*

The main objective of this part of the experiment is to illustrate how sensitive BER is to the mistuning of the PLL free running frequency, for different loop gains.

The parameters that are kept constant are ω_n and ζ, which also implies that the noise bandwidth remains fairly constant provided $K >> \omega_n$.

The PLL free running frequency can be adjusted by the variable resistor R_x (see Fig.6.3). The values for ω_n and ζ was set to 0.01x10^6 rad/sec and 1.0, respectively. The results are presented in Fig.6.6. It indicates that high loop gain of the PLL will lead to smaller sensitivity of BER to a given mistuning of the PLL.

4) *BER vs. Received Optical Power*

The results from the 3 previous experiments show that a small noise bandwidth, high loop gain and a damping factor not smaller than 0.5 are desirable for good performance.

In this part of the experiment, the value for K was again chosen to be high; that is, 1x10^6 rad/sec. For all cases considered except one, the damping factor was chosen to be unity. Signals transmitted were pseudo-random of $10^{20}-1$ bit length. The experimental results are illustrated in Fig.6.7. It shows that the BER performance started to degrade when the noise bandwidth increases, and that it is not much influnced by the values of the damping

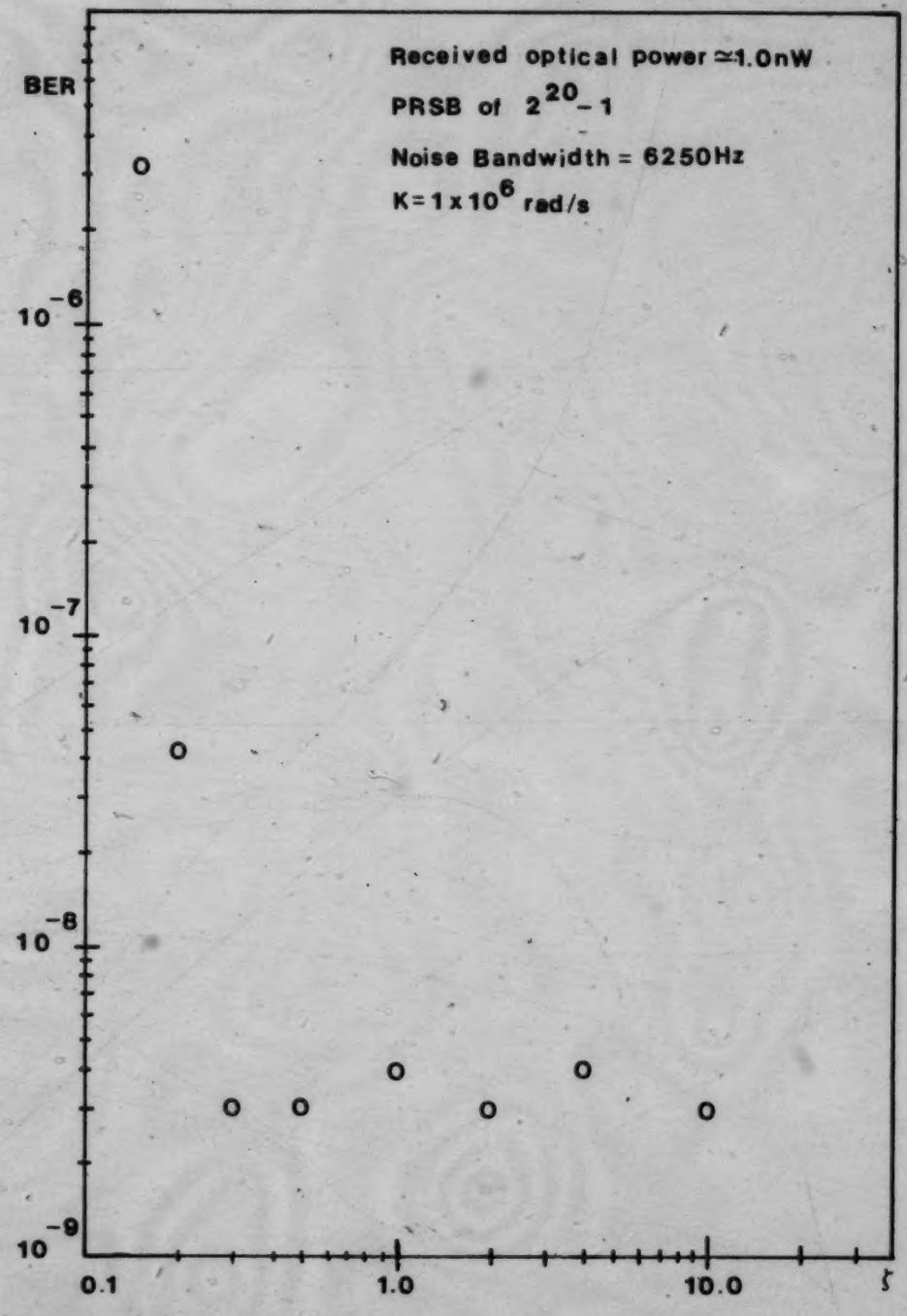


FIG.6.5: BER vs. Damping Factor

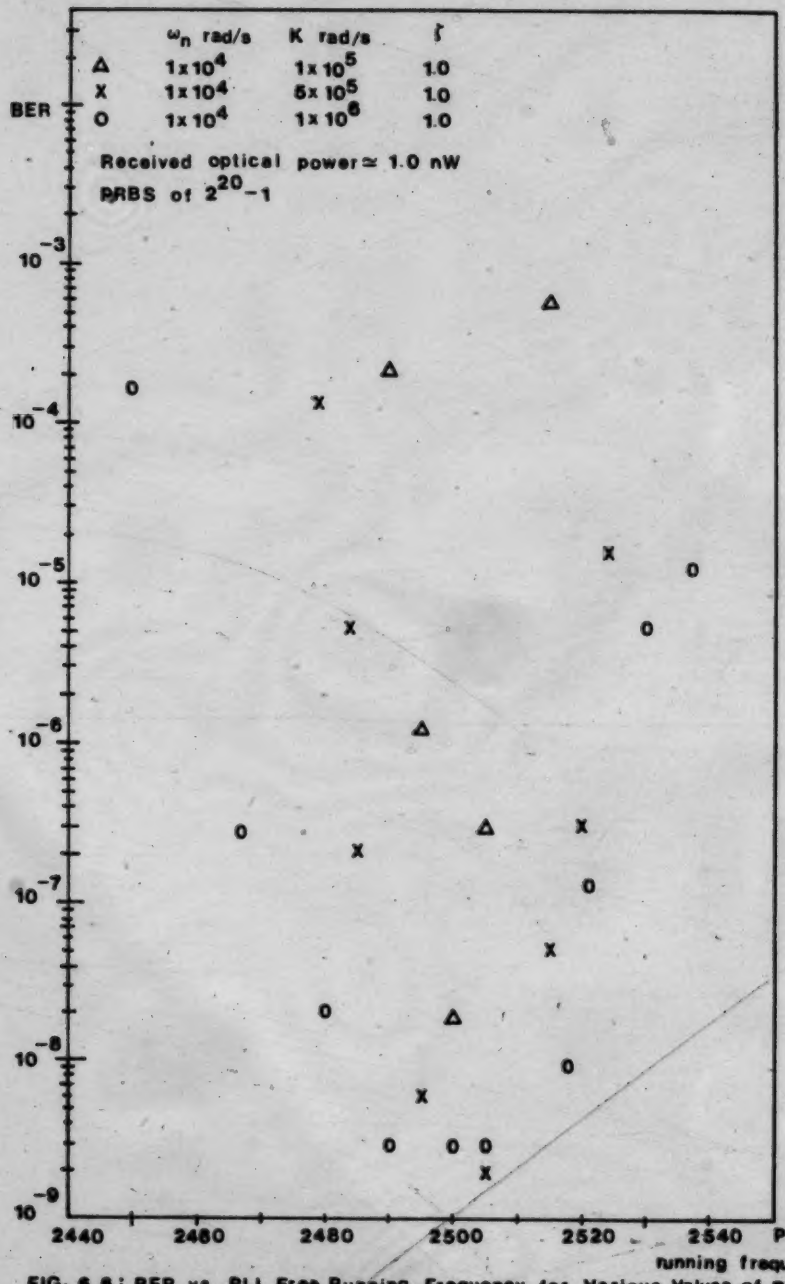


FIG. 6.6 : BER vs. PLL Free Running Frequency for Various Values of PLL Gain

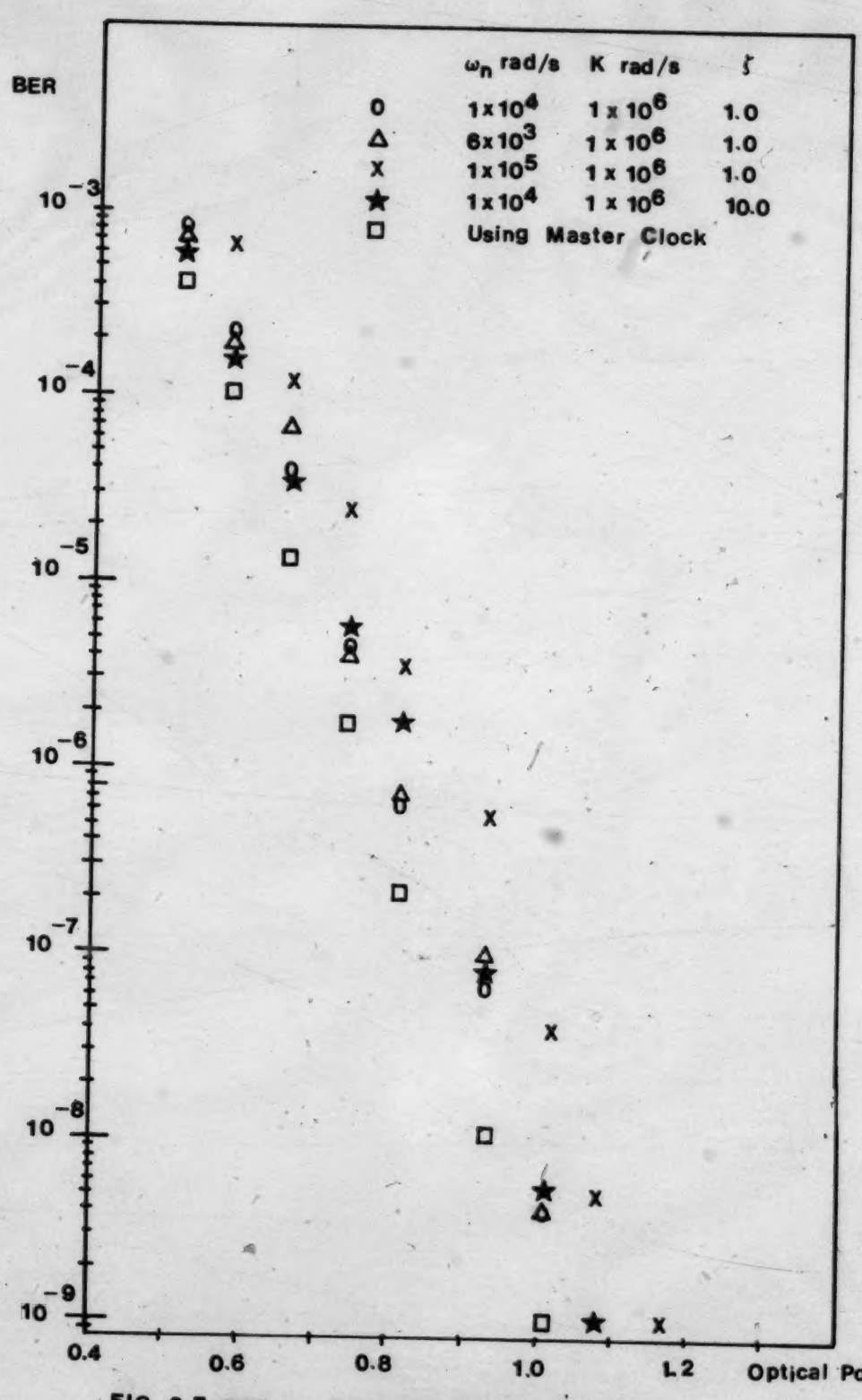


FIG. 6.7: BER vs. Received Optical Power

factor.

5) *Phase Variation with Change of Repetitive Pattern*

A repetitive pattern can be easily generated by using an 8-bit shift register, as shown in Fig.6.8. The block length used should be as long as possible to have as many patterns as possible but not so long that there is so many distinct patterns that the measurement becomes impractical. A block length of 8 bits was chosen as a reasonable value.

Any desired pattern could be stored in the shift register by using the set and reset control of each bit of the shift register, so that either a '0' or a '1' could be store in each bit. The repetitive pattern could be generated by sending the timing signal to the shift register. For example, a 1100000011000000..... repetitive pattern could be generated by first storing a 11000000 pattern into the register and the pattern could be generated by the clock timing. In this way different patterns could be generated. The objective of this experiment is to examine how different data patterns could influence the phase of the recovered timing waveform signal.

In order to measure the change in phase due to different patterns, the master clock is used as the timing reference. The experimental results are illustrated in Table 6.1. These results confirm that the clock phase is dependent on the regularity of the positive rising transitions of the received signal.

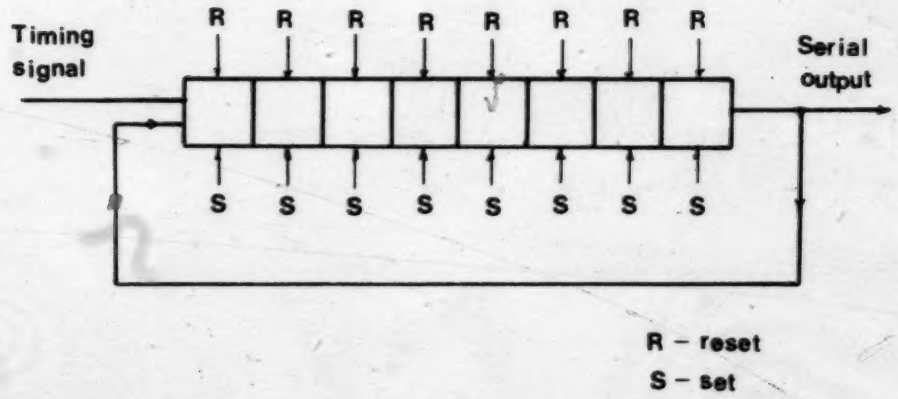
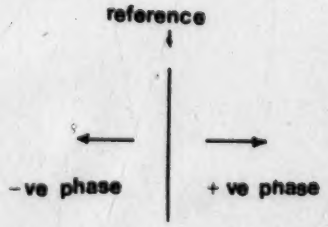


FIG.6.8: A SIMPLE PATTERN GENERATOR USING A SHIFT REGISTER

TABLE 6.1: EFFECTS OF BIT PATTERN ON CLOCK PHASE

Pattern	PWM Pulse	Phase (degree)	Pattern	PWM Pulse	Phase (degree)
10000000	3000	14.4	11010010	2103	-7.2
11000000	2000	15.3	11001100	2020	0 (Reference)
10100000	3300	3.6	11001010	2033	-9
10010000	3100	4.5	10101010	3333	-13.5
10001000	3030	5.4	11111000	2230	-8.1
11100000	2300	0	11110100	2210	-9
11010000	2100	2.7	11110010	2203	-7.2
11001000	2030	1.8	11101100	2320	-9
11000100	2010	0.9	11101010	2333	-11.7
11000010	2003	1.8	11100110	2313	-12.6
10101000	3330	-6.3	11011010	2133	-12.6
10100100	3310	-7.2	11111100	2220	-7.2
11100000	2300	4.5	11111010	2233	-11.7
11101000	2330	-9.9	11110110	2213	-12.6
11100100	2310	-4.5	11101110	2323	-12.6
11100010	2303	-9.0	11111110	2223	-14.4
11011000	2130	-10	11111111	2222	-13.5
11010100	2110	-7.2			

PWM Pulse : 0 - t_0
1 - t_1
2 - t_2
3 - t_3



6.2.4 Discussion of Experimental Results

The experimental results indicate that the system BER performance with self-recovered timing is comparable to that provided by the master clock timing. The good performance can be explained by two reasons:

1) The 4-level PWM signal contains strong timing content which allows easy extraction of its clock signal.

2) A PLL is an efficient noise rejection device. With proper selection of the values of the PLL's parameters, such as the noise bandwidth, the damping factor and the loop gain, it can effectively restrict the phase jitter of the recovered clock.

The results shown in Fig.6.4 point towards the fact that the product B_nT should lie between 0.0005 to 0.01(see Fig.6.4). Alternatively, if we wish to use the parameter "effective Q factor" defined by Roza[57] as

$$Q_{eff} = \frac{\pi}{4TB_n} \qquad (6.16)$$

then, for comparable performance the value of Q_{eff} should be $78.5 < Q_{eff} < 785$, a fairly wide range.

As for the damping factor ζ, the results shown in Fig 6.5 again indicate that the BER is unaffected by ζ for values ≤ 0.25, at which value the timing jitter due to the underdamped response becomes intolerable. It is important to note that this experiment was conducted with a constant noise bandwidth of 6250Hz or $Q_{eff} = 314$ for the various values of ζ.

The most interesting results are the effect of loop gain on BER for a given amount of mistuning. From Fig.6.6, one can easily notice that the PLL with the highest K has the least sensitivity to a given amount of mistuning. The reason is that as K increases, the static phase error of the PLL, or the phase shift in the derived clock signal, becomes smaller. This implies that for a given amount of mistuning, the shifting of the sampling instant from the point of maximun signal eye opening will be less with larger value of K.

The overall system BER performances for various received optical power levels are shown in Fig.6.7, The results have shown to be consistent with the results obtained from the experiments on BER vs 1) noise bandwidth, 2)damping factor and 3)PLL mistuning. The BER

characteristics seem to be close to each other for B_n =6.25KHz and B_n =3.75KHz; also this holds whether ζ =1.0 or ζ =10.0. The BER characteristics start to show marked degradation when the noise bandwidth is increased to B_n =62.5KHz, or Q_{eff} =31.4.

The experimental results in Table 6.1 show the shift in phase of the derived timing clock due to different patterns. The results confirm that the phase relation is not so much dependent on the bit pattern as it is on the pattern of the positive rising edge. In other words, the phase of the derived clock will depend on how often or how regularly the symbols will be with a positive rising transition.

To summarize, the overall system with its self-recovered clock signal can perform almost as well as a system that uses a master clock. This good performance is due to the inherent strong timing content of the PWM signal, and also to the superior qualities of a PLL that can be exploited to perform as an efficient timing extraction device. It is important to note that the range of optimum values for the various parameters is large and hence there is no need for any use of costly and high accuracy components, as long as the specifications of these parameters lie within their optimum range.

Results from this work show that the optical fiber system used in this experiment, though it has shot noise as an additional source of timing jitter, requires no marked difference in the selection of the PLL parameter values for optimum performance as compared with conventional communication system using coaxial cables.

Chapter 7

SUMMARY AND CONCLUSION

The error mechanisms in a multi-level PWM optical fiber communication system have been investigated previously. However, that investigation was based on what has been referred to in this thesis as the "slope theory". This theory is basically an extention of the noise analysis method that is used to determine the SNR in an analog PWM communication system. It characterises the timing error as being chiefly dependent on the noise voltage at the 'slicing' level, and the slope of the falling edge of the received PWM signal. In this thesis we show that the "slope theory" will in general underestimate the BER in a quantised PWM system. The BER may be fairly accurately predicted using a more general method of noise analysis which depends on the noise level and on the signal amplitude level.

An experimental 4-level PWM optical fiber communication system operating at 5 Mbit/s, had been set up prior to the commencement of this work, in order to verify the slope theory. Some experimental measurements had been carried out, but were incomplete. It was the original intention of this thesis to continue the experimental measurements required to verify the slope theory, but instead, the measurements demonstrate the limitations of applicability of the slope theory to quantized PWM system. The experimental measurements have shown a discrepancy between the theoretical calculation and the experimental results. This prompted a reassessment and, subsequently, the replacement of the slope theory by the more general theory, which has been referred to in this thesis as the "amplitude theory". It has been shown in this thesis, both theoretically and experimentally, that the timing error (better known as local error) evaluated by the slope theory can significantly underestimate the system BER, and that the dominant error mechanism is caused by noise at the signal 'ON' and 'OFF' levels, causing incorrect decisions at the decoder. These errors, called global errors, are not dependent on the slopes of the pulse edges but simply on the pulse amplitude. In general, amplitude theory relates errors to the expression $(V_0(t)_s - V_d)/\sigma_T$, where V_d is the 'slicing' voltage level and $V_0(t)_s$ and σ_T are the signal voltage level and square root noise variance, respectively, at the instant of sampling. In order to simplify the computation procedure for the system error rate, the statistical distribution for the channel noise was assumed to be approximately Gaussian. This Gaussian approximation, used in both the slope

and amplitude theories, can be utilised with acceptable accuracy provided that the received optical power is not too small (greater than 0.1nW for the experiments discussed in this thesis).

With the aid of the 4-level PWM experimental system, various BER measurements were carried out. Theoretical error rates using the amplitude theory are in good agreement with the obtained experimental results. The slope theory can still provide a good estimation of timing error calculation provided that: 1)the slope at the sampling instant is approximately the same as that at the 'slicing' level and 2)there is no significant difference in noise variances at the instant of sampling and at the 'slicing' level.

A Multi-level PWM system, as evaluated by the amplitude theory, has no great intrinsic advantage over multi-level PAM, with respect to system BER performance. For a 4-level PWM system at 5 Mbit/s, a BER of 10^{-9} was obtained for a received optical power of approximately 1 nW. However it has two practical advantages. These are that 1)the linear operating range for both the optical transmitter and receiver is not a critical factor and 2)a multi-level PWM signal contains very strong timing information, which facilitates the timing extraction process at the receiver. It is this second advantage that was considered in detail in the later part of the thesis.

One important function of a digital communication receiver is to recover a sufficiently stable clock signal such that precise sampling instants can be generated in order to recover the original message signal. An unstable or jittering clock signal will impair the system BER performance. In other words the BER deteriorates as clock jitter increases. Clock recovery at the receiver is normally a process of extracting a discrete component of the received signal spectrum at the pulse repetition frequency or its higher harmonics. As the spectral distribution of the received signal also contains the continuous spectrum, which tends to cause interference in the timing extraction process, the quality or stability of the recovered clock signal will depend on two major factors, namely: 1)the timing content of the received signal and 2)the characteristics of the timing extraction circuit at the receiver. Spectral analysis of the various pulse modulation schemes shows that asymmetrical PWM signals exhibit a stronger timing content than PAM, PPM, and NRZ or RZ binary signals. In this project, a PLL was used in the design of the timing extraction circuit as it has superior performance as compared to a tuned circuit. As opposed to the characteristics of a tuned circuit, a second-order, high gain PLL has the capability not only of producing signals of consistent amplitude even without the

input excitation, but also of achieving the equivalent of a very narrow-band bandpass filter without the problem of increased static phase error. These properties of the PLL help to reduce the timing jitter, resulting in a stable clock signal.

This thesis has experimentally investigated the optimization of the three major parameters of a PLL in order to produce a clock signal with minimum jitter, as indicated by the system BER performance. These three parameters are: the noise bandwidth, the damping factor and the gain. The utilisation of a second-order PLL with a lag-lead filter instead of a simple RC filter allowed the independent adjustment of these parameters, thus allowing the experimental investigation of their optimum values. The experimental results show that these parameters are not critical and can be chosen over fairly wide operating ranges, to give optimum or near-optimum system BER performance. In our experiments, a second-order PLL with very high loop gain, typically greater than 0.5×10^6 rad/sec, a narrow noise bandwidth of a few hundred times smaller than the signal baud rate and a damping factor not smaller than 0.5, has been shown to provide a sufficiently stable clock signal for optimum system BER performance. This system BER performance was shown to have only a slight degradation as compared to the same system when the receiver was timed directly by the transmitter clock. Therefore, a 4-level PWM optical fiber communication system, though requiring a broader channel bandwidth as compared to a 4-level PAM system, has the major advantage of allowing recovery of a sufficiently stable clock at the receiver with no great difficulty. A multi-level PAM signal not only has weaker timing content but, due to its multi-amplitude signal, needs greater complexity in the circuitry for the timing extraction process.

This thesis has investigated the error mechanisms and the use of the PLL for clock recovery in a 4-level PWM optical fiber communication system. However, further experimental work that could be carried out includes:

1)The system is currently operating at 5 Mbit/s, due to laboratory equipment limitations. It would be commercially attractive to upgrade the system to 44.78 Mbit/s (DS3 standard) and higher bit rates. At higher bit rates, new problems would arise in the design of the clock recovery circuit.

2)An error correction scheme could be incorporated into the receiver to decode the invalid codes (see Fig.3.6).

Methods of clock recovery for conventional communication systems are well established, but this is not yet so for optical fiber communication systems. A theoretical analysis of clock recovery and jitter has been made, particularly by Mengali[56,59,60], but the theoretical results have not been verified experimentally. Further research work could be undertaken in the following areas:

1)Timing jitter can be broadly categorised into random jitter and pattern-dependent jitter. It would be useful to design a jitter measuring instrument that can measure jitter for a transmission system working up to 50 Mbit/s and at the same time having the capability to measure each of the two kinds of jitter separately. Work on such an instrument is under way in the laboratory.

2)With the above jitter measuring instrument, the effects of system parameters, such as shot noise, thermal noise, and the various parameters of the PLL on the two catagories of timing jitter could be investigated in greater depth.

3)Theoretical work has been done to compute the variance of the jitter in a timing recovery circuit using a tuned circuit for a binary PCM optical fiber transmission system[59]. Optical pulses with Gaussian and Exponential shapes were used in the computation. An experimental system could be set up to verify this theoretical work. A PLL could be used in place of the tuned circuit and a comparison of the system performance could be made.

4) Surface Acoustic Wave (SAW) filter based timing recovery circuits have recently attracted increasing interest for data regeneration in high bit rate digital transmission systems[61,62]. For bit rates above 247Mbits/s the design of the PLL, particularly that for the monolithic PLL, becomes difficult[62]. A SAW filter whose electrical characteristics are similar to that of a tuned circuit has the advantages of having very high Q factor (500 to 1100)[62], simple circuitry and simple implementation. However, it is costly and still shares many of the problems suffered by a tuned circuit (section 4.3.3). A very high bit rate optical fiber system (above 50 Mbits/s) using the PLL and the SAW filter based timing recovery circuits, could be set up. A comparison of their performance, and improvements of these two methods should be investigated.

It is hoped the work in this thesis on error mechanisms will lay the foundation for future work on error rate calculations in multi-level PWM communication systems, and that it will generate interest both in future theoretical and experimental investigations in this area.

APPENDIX A

Spectra of PAM with Sinusoidal Modulation

The following is the derivation of the spectrum for an analog PAM modulated by a sine wave.

Consider the modulating signal s(t) such that,

$$s(t) = A\cos 2\pi f_s t$$

$$c_\delta(t) = \sum_{m=-\infty}^{\infty} \delta(t-mT) = \frac{1}{T}\sum_{m=-\infty}^{\infty} \cos 2\pi m f_0 t \qquad (A.1)$$

$$since\ x_\delta(t) = s(t)c_\delta(t)$$

$$x_\delta(t) = \frac{A}{T}\sum_{m=-\infty}^{\infty} \frac{1}{2}\{\cos 2\pi(f_s + mf_0)t + \cos 2\pi(f_s - mf_0)t\}$$

$$= \frac{A}{T}\sum_{m=-\infty}^{\infty} \cos 2\pi(f_s + mf_0)t \qquad (A.2)$$

The desired sequence of flat-top pulses is obtained by summing the contribution of all of the trains of short pulses over the range $-t_o/2$ to $t_o/2$.

$$x_1(t) = \frac{A}{T}\sum_{m=-\infty}^{\infty} \int_{-t_o/2}^{t_o/2} \cos 2\pi(f_s + mf_0)(t - \tau)d\tau \qquad (A.3)$$

$$Let\ 2\pi(f_s + mf_0) = N$$

Therefore the integral part of $x_1(t)$ will be,

$$\int_{-t_o/2}^{t_o/2} \cos N(t-\tau)\,d\tau$$

$$= \frac{2}{N} \sin \frac{Nt_o}{2} \cos(Nt) \qquad (A.4)$$

$$x_1(t) = \frac{At_o}{T} \sum_{m=-\infty}^{\infty} \frac{\sin(Nt_o/2)}{Nt_o/2} \cos Nt \qquad (A.5)$$

where $N = 2\pi(mf_0 + f_s)$

Adding a d.c. component to $x_1(t)$,

$$x_1(t) = \frac{At_o}{T} \sum_{m=-\infty}^{\infty} \frac{\sin(Nt_o/2)}{Nt_o/2} \cos Nt + D\frac{t_o}{T} \sum_{m=-\infty}^{\infty} \frac{\sin(mt_o\pi/T)}{mt_o\pi/T} e^{j2\pi mf_0 t} \qquad (A.6)$$

where D is a multiplier for the d.c. component.

Hence, PAM with $t_o = T/2$ (that is RZ format) has distinctive line spectrum at its pulse repetition frequency.

APPENDIX B

Comparing Timing Content of the PWM, RZ Binary, and NRZ Code Format

Consider the random pulse train depicted in Fig.B1. The spectrum of a random sequence of rectangular pulses can be computed by using the autocorrelation method. Assume here for simplicity that the 4-level PWM signals are random and that the random pulse train in Fig.B1a is generated from the leading edge of these PWM pulses. The autocorrelation function is defined by ,

$$R(\tau) = \lim_{T\to\infty} \frac{1}{T} \int_{-T/2}^{T/2} f(t)f(t+\tau)d\tau \qquad (B.1)$$

If the 4-level PWM signals are truely random, then the probability of occurrence of a pulse in any one time slot is 3/4 so that

$$R(0) = \frac{E^2 t_o}{T} \cdot \frac{3}{4} \qquad (B.2)$$

For τ lying between t_o and $T-t_o$, one of the two terms in the product $f(t)f(t-\tau)$ will be zero, giving

$$R(\tau) = 0$$

When $\tau = nT$, both terms may occur with probability of 3/4 so that

$$R(nT) = \frac{E^2 t_o}{T} \cdot \frac{3}{4} \cdot \frac{3}{4} = \frac{9}{16} \frac{E^2 t_o}{T} \qquad (B.3)$$

The autocorrelation for the random pulse train consists of a non-periodic component $R_1(\tau)$ and a periodic component $R_2(\tau)$ (see Fig.B1b and Fig.B1c).

Corresponding to the non-periodic part, the energy spectrum of the signal contains a continuous distribution given by

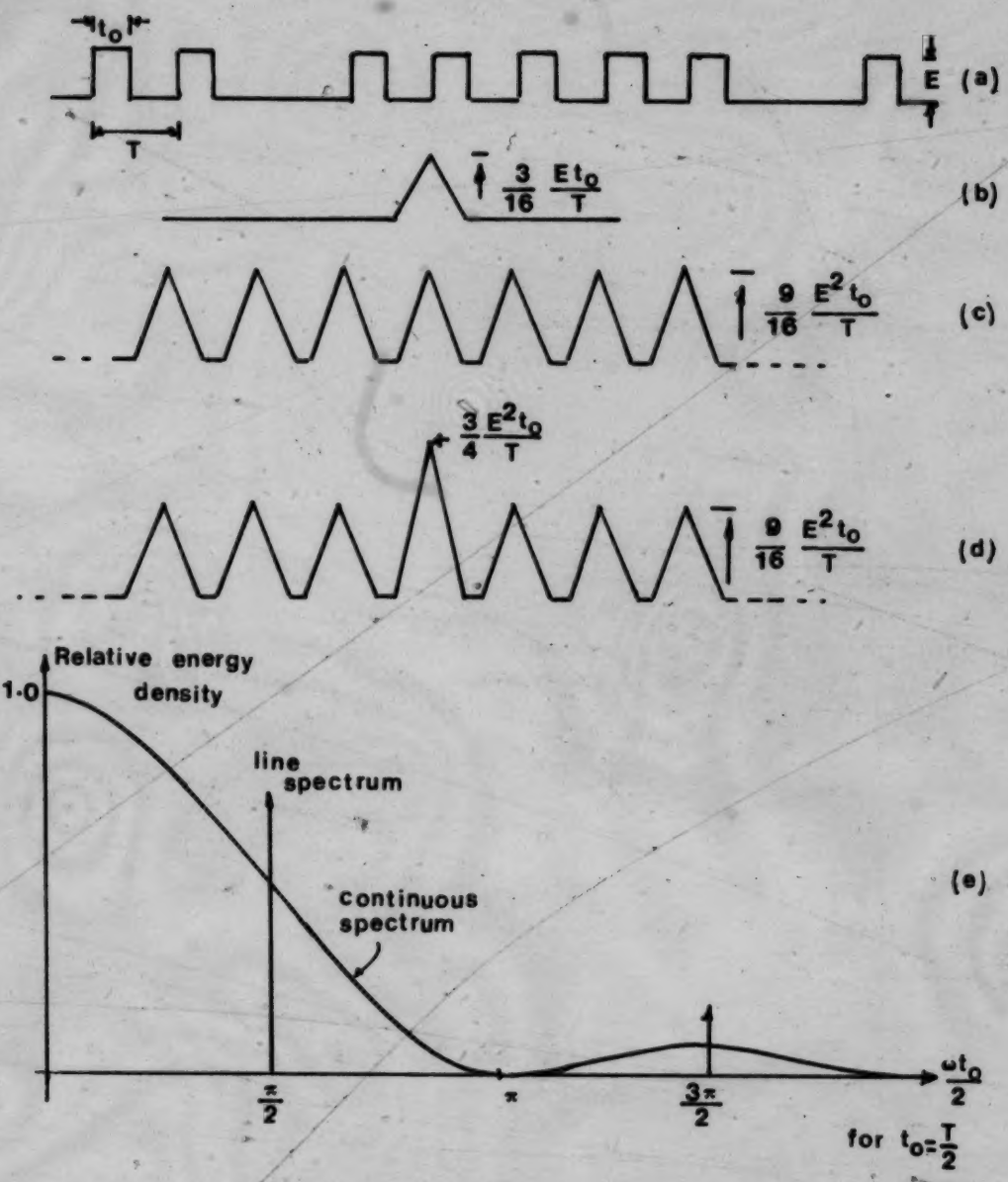


FIG. B1: a Random Pulse Train

b Autocorrelation for Non-periodic Part $R_1(\tau)$

c Autocorrelation for Periodic Part $R_2(\tau)$

d Sum of $R_1(\tau)$ and $R_2(\tau)$

e Energy Spectrum

$$F_1(f) = \int_{-\infty}^{\infty} R_1(\tau)\cos(2\pi f\tau)\,d\tau$$

as $R_1(\tau)$ is an even function.

as $R_1(\tau)$ is an even function. This yield a continuous spectrum given by

$$F_1(f) = \frac{3}{16} \cdot E^2(t_o/T)^2 T(\mathrm{sinc}\pi f t_o)^2 \qquad (B.4)$$

The periodic part $R_1(\tau)$ then leads to a line spectrum.

$$F_2(f) = \sum_{n=-\infty}^{\infty} a_n^2 \cos(2\pi nt/T)$$

$$\text{where } a_n^2 = \frac{1}{T}\int_{-T/2}^{T/2} R_2(\tau)e^{-j2\pi n\tau/T}\,d\tau$$

This yield a line spectrum

$$F_2(f) = \frac{9}{16} E^2(t_o/T)^2\{\sin n\pi f_0 t_o/(n\pi f_0 t_o)\}^2 \qquad (B.5)$$

If $t_o = T/2$, then

$$F_1(f) = \frac{3}{64} E^2 T \frac{\sin(\omega t_o/2)}{\omega t_o/2} \qquad (B.6)$$

$$F_2(f) = \frac{9}{64} E^2 \frac{\sin(n\pi/2)}{n\pi/2} \qquad (B.7)$$

The same derivation can be carried out for RZ binary code format where the probability of occurrence of a pulse in any time slot is 1/2.

$$F_1(f) = E^2\{t_0/(2T)\}^2 T\{\sin\pi f t_o/(\pi f t_o)\}^2 \qquad (B.8)$$

$$F_2(f) = E^2\{t_o/(2T)\}^2\{\sin n\pi f_0 t_o/(n\pi f_0 t_o)\}^2 \qquad (B.9)$$

Assume a NRZ binary code format signal (that is full width rectangular pulses) is applied to a single-shot monostable to produce pulses of amplitude E and duration t_o on every leading or positive-going transition. Since the probability of a positive transition is now only 1/4, the line spectrum will be

$$F_2(f) = \frac{1}{16} E^2 (t_o/T)^2 \{sinn\pi f_0 t_o/(n\pi f_0 t_o)\}^2 \qquad (B.10)$$

Hence, the line spectrum with a fundamental component at the pulse reptition frequency in terms of voltage are given by

4-level PWM: $v = \frac{3E}{4\pi} sin(\frac{\pi t_o}{T})$

Binary RZ code format: $v = \frac{E}{2\pi} sin(\frac{\pi t_o}{T})$

Binary NRZ code format: $v = \frac{E}{4\pi} sin(\frac{\pi t_o}{T})$

It can be seen, therefore, that the 4-level PWM has the strongest timing content.

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